

Features

- Built-in an 8-bit CPU core
- Built-in 128~208 bytes of data RAM
- Built-in 0~1024KB user data ROM
- Built-in 16K~60KB program ROM
- On-chip RC oscillator or crystal oscillation clock input
- 32kHz internal RC oscillator
- Illegal address reset
- Maximum of 24 programmable I/O pins
- Internal RC oscillator for Timer or WDT
- Watch-dog timer (WDT)
- Power saving STOP & HALT modes
- Maximum of 2*16-bit (or 8-bit) & 2*8-bit timers
- External interrupt input
- I/O State Change wake-up option for all of I/O port
- Operating voltage 2.4V – 5.4V
- Programmable R-option for PA4~7 & PB0~7
- Support 32768Hz crystal oscillator share with Port A
- 1ms interrupt (@ Fsys=2MHz)

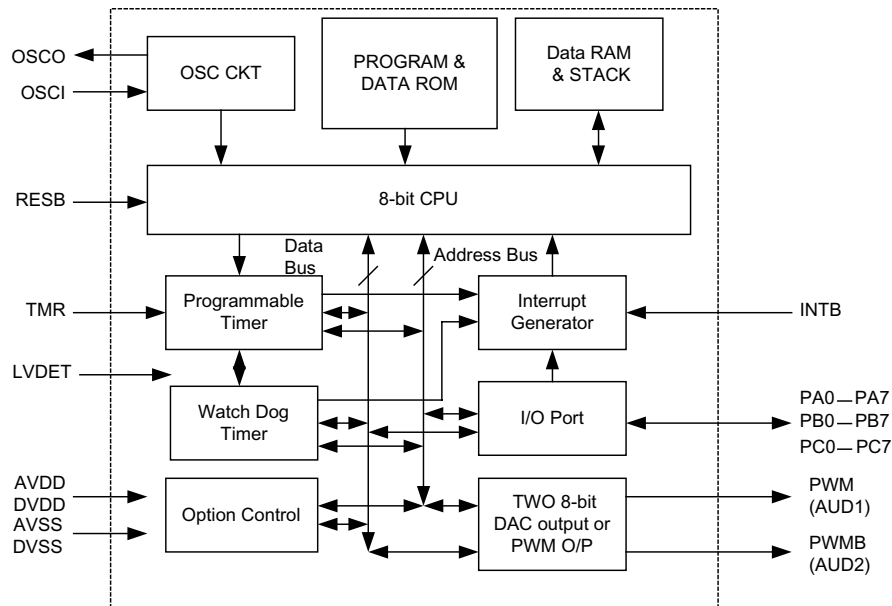
General Description

JA23000 series is a series of 14 to 340 seconds (S.R.=6kHz, 4-bit ADPCM) single chip voice synthesizer IC with a PWM Direct Drive circuit or AUD output for transistor application, JA23000 series contains an 8-bit Micro-Controller Units (MCU), 12~24 programmable general I/Os, 16KB~60KB Program ROM, Special register, 0~1024KB Data ROM, 4 CHs of current type DAC or 2 CHs PWM output for voice output, 128~208

bytes of user data RAM and 2*16-bit (or 8-bit) & 2*8-bit Timers. The advanced sub-micron CMOS process technology ensures JA23000 series high performance, high reliability and sophisticated functionalities. In addition, this chip also provides high sink current port pins, multi external interrupt pins, Low Voltage Detector (LVD) function, and multi oscillator options. JA23000 series offers the best cost/performance ratios, as a controller, for the industry applications.

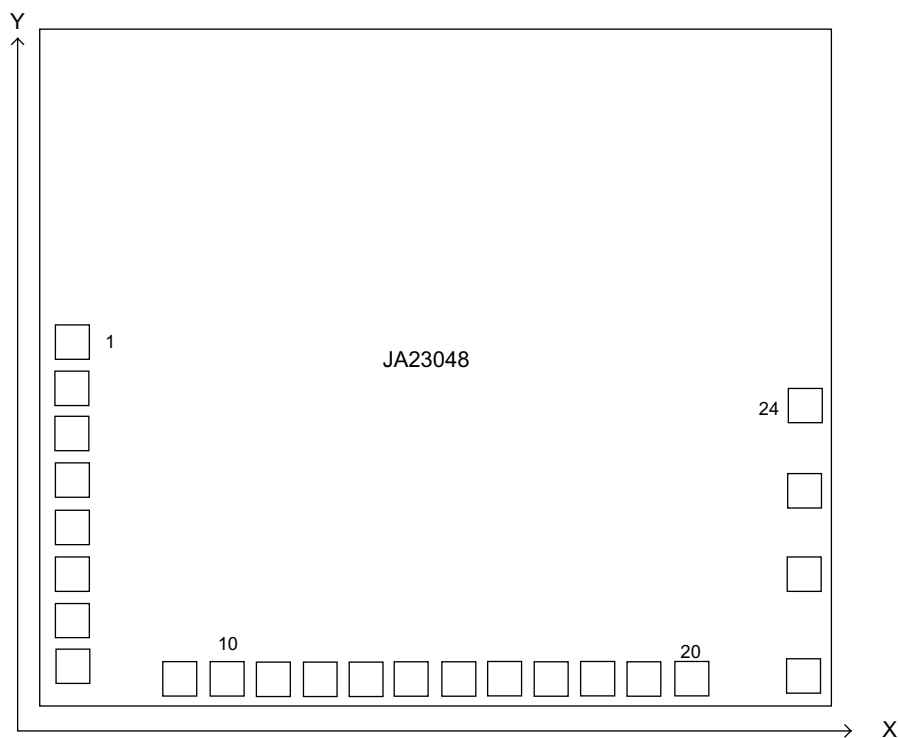
Selection Table

Part No.	JA23048	JA23060	JA23384	JA23512	JA23768	JA231K0
I/O	12	12	24	24	24	24
PROM	48KB	60KB	16KB	16KB	16KB	16KB
DROM	0	0	384KB	512KB	768KB	1024KB
RAM	128B	128B	208B	208B	208B	208B
Timer (Bits * No.)	8b*2	8b*2	16*2 & 8*2	16*2 & 8*2	16*2 & 8*2	16*2 & 8*2
PWM	V	V	V	V	V	V
DAC		V	V	V	V	V

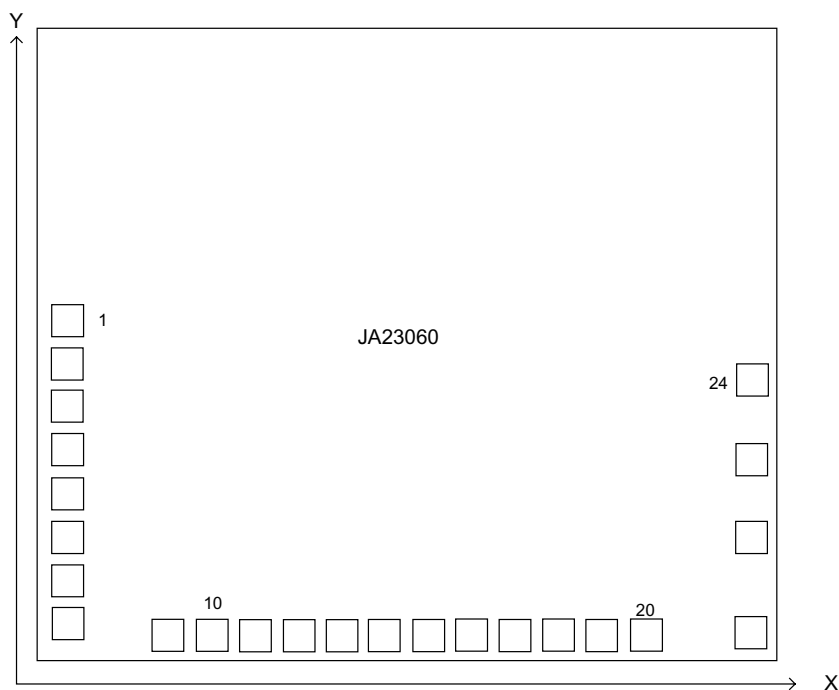
Block Diagram

Pin Assignment

Pin Name	I/O	Internal	Description
TMR	I/O	—	Timer counter input or timer clock output by pin option.
RESB	I	Pull Hi	System input, active low.
DVSS, AVSS	—	—	Negative power supply.
PA0 — PA7 PB0 — PB7 PC0 — PC7	I/O	Pull Hi (*)	Port I/O pins can be configured as input, output, or interrupt input pin. Some pins can configure for special function. Please refer to the I/O configuration description.
DVDD, AVDD	—	—	Positive power supply.
OSCO	O	—	In XTAL mode, it connects to an external XTAL between OSCI and OSCO. In RC mode, its output is the F _{sys} /4.
OSCI	I	—	In XTAL mode, it connects to an external XTAL between OSCI and OSCO. In RC mode, it connects to an external oscillator resistor between OSCI and VDD. Meanwhile, the pin can be used as a external clock input.
INTB	I	Pull Hi	INT input pin by user program option.
PWM(AUD1), PWMB(AUD2)	O	PMOS (AUD1,2)	Current type DAC output for driving external transistors or driving speaker directly by mask option.
LVDET	I	—	Low voltage detection pin. Connect a resistor between LVDET and VSS to adjust the low battery detection.

(*) : The pull high resistor with or without is optional by user program.

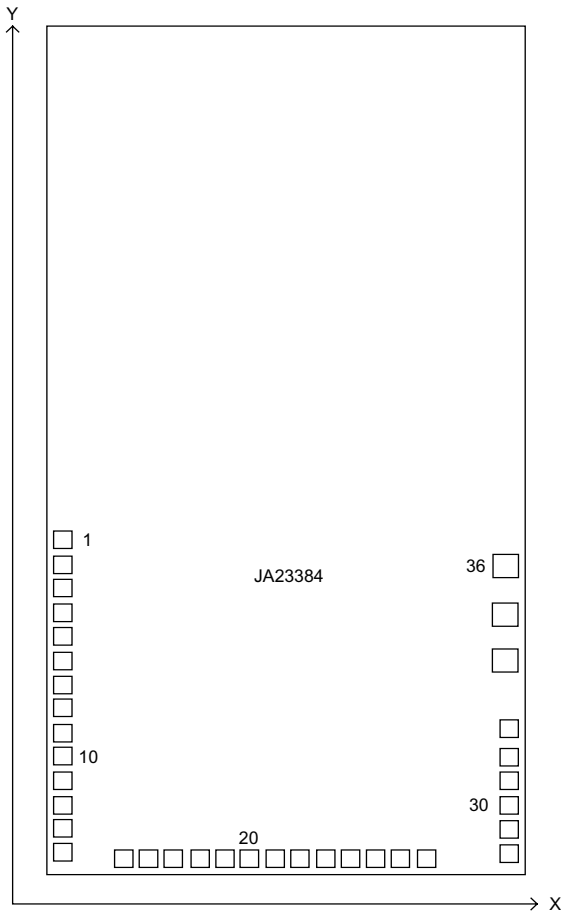
Pad Diagram & Pad Location
● JA23048


Pad No.	Pad Name	X(um)	Y(um)	Pad No.	Pad Name	X(um)	Y(um)
1	PA7	70	857.7	13	VDD	755.1	70
2	PA6	70	747.9	14	VSS	864.9	70
3	PA5	70	638.1	15	LVDET	974.7	70
4	PA4	70	528.3	16	INTB	1084.5	70
5	PA3	70	418.5	17	TMR	1194.3	70
6	PA2	70	308.7	18	RESB	1304.1	70
7	PA1	70	198.9	19	OSCO	1413.9	70
8	PA0	70	89.1	20	OSCI	1523.7	70
9	PB0	315.9	70	21	VDD	1787.6	71.1
10	PB1	425.7	70	22	PWM	1787.6	311.55
11	PB2	535.5	70	23	VSS	1787.6	510.3
12	PB3	645.3	70	24	PWMB	1787.6	709.05
Chip Size : 1858.00 x 1587.25 (μm) ²							

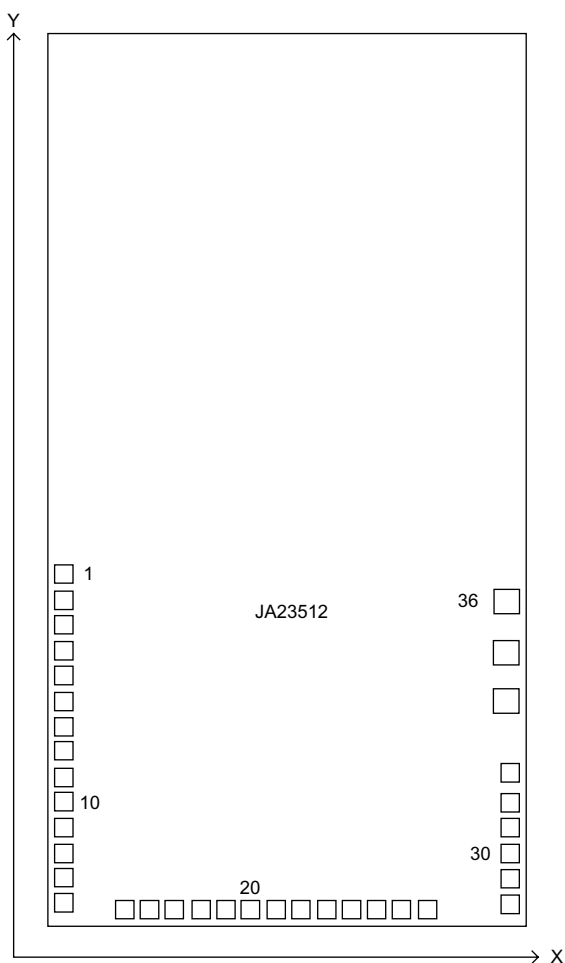
● JA23060


Pad No.	Pad Name	X(um)	Y(um)	Pad No.	Pad Name	X(um)	Y(um)
1	PA7	70	857.7	13	VDD	755.1	70
2	PA6	70	747.9	14	VSS	864.9	70
3	PA5	70	638.1	15	LVDET	974.7	70
4	PA4	70	528.3	16	INTB	1084.5	70
5	PA3	70	418.5	17	TMR	1194.3	70
6	PA2	70	308.7	18	RESB	1304.1	70
7	PA1	70	198.9	19	OSCO	1413.9	70
8	PA0	70	89.1	20	OSCI	1523.7	70
9	PB0	315.9	70	21	VDD	1787.6	71.1
10	PB1	425.7	70	22	PWM	1787.6	311.55
11	PB2	535.5	70	23	VSS	1787.6	510.3
12	PB3	645.3	70	24	PWMB	1787.6	709.05
Chip Size : 1858.00 x 1587.25 (μm) ²							

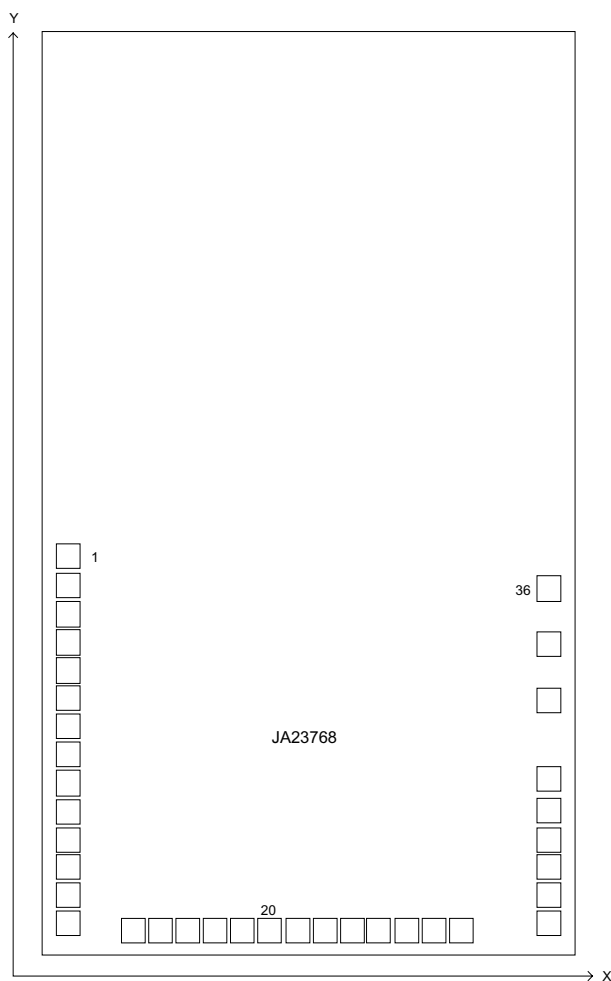
● **JA23384**



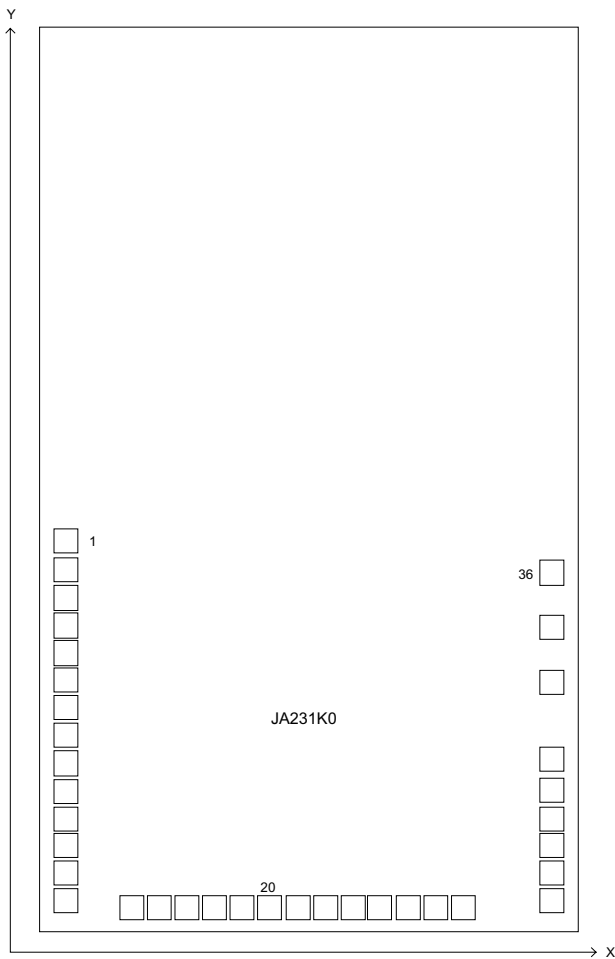
Pad No.	Pad Name	X(um)	Y(um)
1	PA7	70	1530.3
2	PA6	70	1420.1
3	PA5	70	1309.9
4	PA4	70	1199.7
5	PA3	70	1089.5
6	PA2	70	979.3
7	PA1	70	869.1
8	PA0	70	758.9
9	PB0	70	648.7
10	PB1	70	538.5
11	PB2	70	428.3
12	PB3	70	318.1
13	PB4	70	207.9
14	PB5	70	97.7
15	PB6	335.2	70
16	PB7	445.4	70
17	PC0	555.6	70
18	PC1	665.8	70
19	PC2	776	70
20	PC3	886.2	70
21	PC4	996.4	70
22	PC5	1106.6	70
23	PC6	1216.8	70
24	PC7	1327	70
25	VDD	1437.2	70
26	VSS	1547.4	70
27	LVDET	1657.6	70
28	INTB	2015.9	97.7
29	TMR	2015.9	207.9
30	RESB	2015.9	318.1
31	OSCO	2015.9	428.3
32	OSCI	2015.9	538.5
33	VDD	2015.9	667.7
34	PWM	2015.9	972.9
35	VSS	2015.9	1190.2
36	PWMB	2015.9	1407.5
Chip Size : 2086.1 x 3883.75 (μm) ²			

● JA23512


Pad No.	Pad Name	X(um)	Y(um)
1	PA7	70	1530.3
2	PA6	70	1420.1
3	PA5	70	1309.9
4	PA4	70	1199.7
5	PA3	70	1089.5
6	PA2	70	979.3
7	PA1	70	869.1
8	PA0	70	758.9
9	PB0	70	648.7
10	PB1	70	538.5
11	PB2	70	428.3
12	PB3	70	318.1
13	PB4	70	207.9
14	PB5	70	97.7
15	PB6	335.2	70
16	PB7	445.4	70
17	PC0	555.6	70
18	PC1	665.8	70
19	PC2	776	70
20	PC3	886.2	70
21	PC4	996.4	70
22	PC5	1106.6	70
23	PC6	1216.8	70
24	PC7	1327	70
25	VDD	1437.2	70
26	VSS	1547.4	70
27	LVDET	1657.6	70
28	INTB	2015.9	97.7
29	TMR	2015.9	207.9
30	RESB	2015.9	318.1
31	OSCO	2015.9	428.3
32	OSCI	2015.9	538.5
33	VDD	2015.9	667.7
34	PWM	2015.9	972.9
35	VSS	2015.9	1190.2
36	PWMB	2015.9	1407.5
		Chip Size : 2086.1 x 3883.75 (μm) ²	

● JA23768


Pad No.	Pad Name	X(um)	Y(um)
1	PA7	70	1530.3
2	PA6	70	1420.1
3	PA5	70	1309.9
4	PA4	70	1199.7
5	PA3	70	1089.5
6	PA2	70	979.3
7	PA1	70	869.1
8	PA0	70	758.9
9	PB0	70	648.7
10	PB1	70	538.5
11	PB2	70	428.3
12	PB3	70	318.1
13	PB4	70	207.9
14	PB5	70	97.7
15	PB6	335.2	70
16	PB7	445.4	70
17	PC0	555.6	70
18	PC1	665.8	70
19	PC2	776	70
20	PC3	886.2	70
21	PC4	996.4	70
22	PC5	1106.6	70
23	PC6	1216.8	70
24	PC7	1327	70
25	VDD	1437.2	70
26	VSS	1547.4	70
27	LVDET	1657.6	70
28	INTB	2015.9	97.7
29	TMR	2015.9	207.9
30	RESB	2015.9	318.1
31	OSCO	2015.9	428.3
32	OSCI	2015.9	538.5
33	VDD	2015.9	667.7
34	PWM	2015.9	972.9
35	VSS	2015.9	1190.2
36	PWMB	2015.9	1407.5
Chip Size : 2086.10 x 5810.15 (μm) ²			

● JA231K0


Pad No.	Pad Name	X(um)	Y(um)
1	PA7	70	1530.3
2	PA6	70	1420.1
3	PA5	70	1309.9
4	PA4	70	1199.7
5	PA3	70	1089.5
6	PA2	70	979.3
7	PA1	70	869.1
8	PA0	70	758.9
9	PB0	70	648.7
10	PB1	70	538.5
11	PB2	70	428.3
12	PB3	70	318.1
13	PB4	70	207.9
14	PB5	70	97.7
15	PB6	335.2	70
16	PB7	445.4	70
17	PC0	555.6	70
18	PC1	665.8	70
19	PC2	776	70
20	PC3	886.2	70
21	PC4	996.4	70
22	PC5	1106.6	70
23	PC6	1216.8	70
24	PC7	1327	70
25	VDD	1437.2	70
26	VSS	1547.4	70
27	LVDET	1657.6	70
28	INTB	2015.9	97.7
29	TMR	2015.9	207.9
30	RESB	2015.9	318.1
31	OSCO	2015.9	428.3
32	OSCI	2015.9	538.5
33	VDD	2015.9	667.7
34	PWM	2015.9	972.9
35	VSS	2015.9	1190.2
36	PWMB	2015.9	1407.5
Chip Size : 2086.10 x 5810.15 (μm) ²			

Memory

• Memory Mapping

Address	Definition
00h	POWERC (W)
01h	INTC (R/W)
02h	INTF (R/W)
03h	WDTCLR (W)
04h	WDTC (R/W)
05h	TMR0H (R/W)
06h	TMR0L (R/W)
07h	TMR0C (R/W)
08h	TMR1H (R/W)
09h	TMR1L (R/W)
0Ah	TMR1C (R/W)
0Bh	PA (R/W)
0Ch	PAC (R/W)
0Dh	PAR (R/W)
0Eh	PB (R/W)
0Fh	PBC (R/W)
10h	PBR (R/W)
11h	PC(R/W)
12h	PCC(R/W)
13h	Not used
14h	Not used
15h	Not used
16h	Not used
17h	Not used
18h	Not used
19h	VOLC
1Ah	DA1 (WR)
1Bh	DA2 (WR)
1Ch	DA3 (WR)
1Dh	DA4 (WR)
1Eh	CROMCONT (W)
1Fh	CROMADD (R/W)
20h ~ 2Ah	Special RAM reserved for further expanding for setting internal as internal register
2Bh	TIMER2L (R/W)
2Ch	TIMER2C (R/W)
2Dh	TIMER3L (R/W)
2Eh	TIMER3C (R/W)
30h ~ FFh	General purpose Data Memory & Stack
100h ~ 0FFFh	Reserved used
1000h ~ FFFFh	User Program (16K~60KB) Note : Max 0.5KB for testing program

- The low nibble of VOLC controls the AUD1 & the high nibble of VOLC controls the AUD2 (DAC output only.)

- Data RAM**

Total of 256 bytes of RAM (including the stack, and special register) is available from \$00h to \$FFh. The stack begins at the address \$FFh and proceeds down to \$00h.
 For JA23048 & JA23060 : 128B (80h – FFh)
 For JA23384 – JA231K0 : 208B (30h – FFh)
 The address of 00h – 2Fh are designed for special registers.

- Program ROM**

The JA23000 series includes the Max. of 60K bytes of user ROM which located from \$1000h to \$FFFFh. The 0.5K bytes of internal test ROM is for testing program. The PROM location of various bodies is presented as follows :

For JA23048 (48KB) : 4400h – FFFFh (4000h – 43FFh for testing program)
 For JA23060 (60KB) : 1400h – FFFFh (1000h – 13FFh for testing program)
 For JA23384 – JA231K0 (16KB) : C400h – FFFFh (C000h – C3FFh for testing program)

- Data ROM**

To write the address expander control register of CROMCONT, CROMADD can access max. of 1024KB data. The address from \$00000 to \$FFFFFF. The DROM location of various bodies is illustrated as follows :

Body	JA23384	JA23512	JA23768	JA231K0
DROM size	384KB	512KB	768KB	1024KB
DROM Address	00000h 5FFFFh	00000h 7FFFFh	00000h BFFFFh	00000h FFFFFFh

- NMI, Reset, IRQ vectors**

The address of NMI, RESET and IRQ are located from \$FFFAh to \$FFFFh. The interrupt vectors should be specified in the program as follows :

```

ORG $FFFA
JMP NMI_VECTOR      ;($FFFA, $FFFB)
JMP RESET_VECTOR   ;($FFFC, $FFFD)
JMP INT_VECTOR     ;($FFFE, $FFFF)
  
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- Stack Pointer**

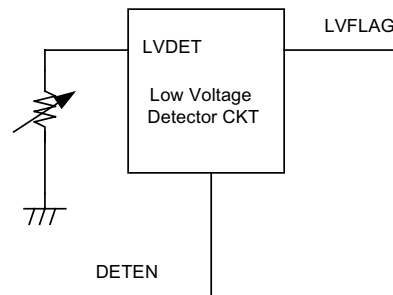
The stack pointer is set from \$FFh after power on.

Power configuration

The JA23000 series provide two power saving mode, one is the HALT mode and the other is the STOP mode. When writing "1" to the HALT bit, the system will enter the HALT mode and the system clock will stop whereas the internal RC will free run continuously. The timer overflow, WDT overflow, and external interrupt will wakeup the system. When writing "1" to the STOP bit, the system will enter the STOP mode and the system clock, internal RC oscillator will be stop. Only the external interrupt (INT or PX change state) can wakeup the system. When the system is overflow, the HALT and STOP bit will be cleared to "0" automatically.

When writing "1" to the DADIS bit, the DAC output will be disabled.

When the DETEN bit is written as "1", then the low battery detector circuit will be enabled, and if the low battery is detected (set by external R), the LVFLAG will be set to "1". Otherwise, this bit is set to "0". After writing the DETEN bit, the user must insert 2 NOP instructions, and then to read the stable LVFLAG data.



POWERC

Register	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
POWERC	00h	LVFLAG	DETEN	—	STOP	—	—	DADIS	HALT

In the HALT mode, the 32K(PA or WDT) is On & Fosc is OFF. In the STOP mode, the 32K(PA or WDT) & Fosc are all OFF.

I/O configuration

Maximum of 24 I/Os (grouped into 3 I/O ports, PA, PB, and PC) are provided. All of these I/O ports can be used as input and output operations. For input operation, these ports are non-latched and for output operation all the data are latched and remain unchanged till the output latch is re-written.

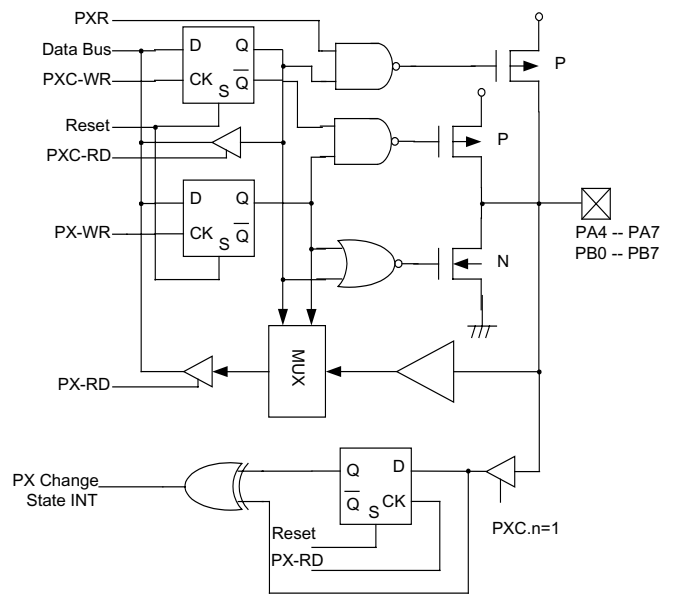
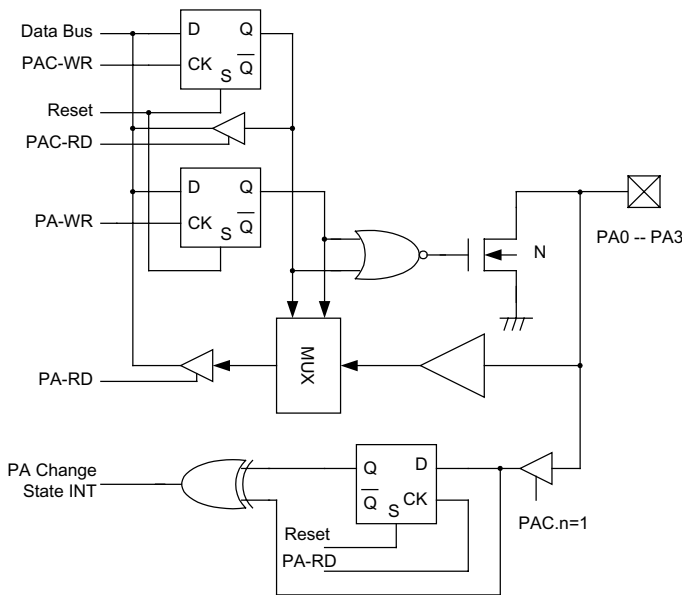
Each I/O line has its own control register (PAC, PBC, and PCC) to control the input/output configuration. If the global interrupt(INTC.0) is disabled and the corresponding I/O interrupt(INTC.4; INTC.5 & INTC.6) is enabled, it will activate the system and its corresponding flag will be set when the corresponding I/O state is changed.

Part No.	I/O	Port A	Port B	Port C
JA231K0	24	8	8	8
JA23768	24	8	8	8
JA23512	24	8	8	8
JA23384	24	8	8	8
JA23060	12	8	4	
JA23048	12	8	4	

PA Configuration

Label	Address	Function	R/W	Default
PA	0Bh	PA data input/output	R/W	FF
PAC	0Ch	PA direction control, 1=input 0=output	R/W	FF
PAR	0Dh	PA pull-high resistor option, 1=With, 0=Without	R/W	FX

1. The PA0 – PA3 they are defined as NMOS open drain output only when PAC is set as output mode.
2. The PA0 – PA3 without pull-high resistor in input mode.



PB Configuration

Label	Address	Function	R/W	Default
PB	0Eh	PB data input/output	R/W	FF
PBC	0Fh	PB direction control, 1=input 0=output	R/W	FF
PBR	10h	PB pull-high resistor option, 1=With, 0=Without	R/W	FF

1. Its diagram is shown above. The output mode (PB0 — PB7) is the same as PA4 — PA7.
2. The pull-high resistor will be disabled automatically when port is programmed as output mode.

PC Configuration

Label	Address	Function	R/W	Default
PC	11h	PC data input/output	R/W	FF
PCC	12h	PCC direction control, 1=input 0=output	R/W	FF

1. The internal pull high resistor of PC can be enabled or disabled by mask option.
2. The pull-high resistor will be disabled automatically when port is programmed as output mode.

Timer

There are 4 sets of programmable timer in JA23000 series, they are TMR0 (05h, 06h & 07h), TMR1 (08h, 09h & 0Ah), TMR2 (2Bh & 2Ch) & TMR3 (2Dh & 2Eh).

Part No.	TMR0	TMR1	TMR2	TMR3
JA231K0	16-bit	16-bit	8-bit	8-bit
JA23768	16-bit	16-bit	8-bit	8-bit
JA23512	16-bit	16-bit	8-bit	8-bit
JA23384	16-bit	16-bit	8-bit	8-bit
JA23060	8-bit	8-bit		
JA23048	8-bit	8-bit		

Note : The TMR0 and TMR1 can be selected as 16-bit or 8-bit mode by mask option.

TMR0H, TMR0L (05h, 06h) & TMR0C (07h)

The TMR0 is a programmable 16-bit/8-bit count-up counter. The counter registers are named as TMR0L (06h) & TMR0H (05h). The clock source may come from Fosc/4, internal RC clock or external. The TMR0C is its control register and the default value is 00. The definition of TMR0C is listed below.

Labels	Bits	Function
TON0 (TMR0)	0	Timer0 enable/disable definition bit 0 = Disable; 1 = Enable
TS0, TS1, TS2	1 - 3	Timer clock source selection bits
—	4	Reserved, not used
TMR/WDT	5	To define the clock source is with pre-scale counter 0: Timer 1: WDT
TM0 TM1	6, 7	To define the operation mode 00 = Timer mode (internal system clock; Fosc/4) 01 = Timer mode (internal RC clock) 10 = Event count mode (external clock) 11 = Timer mode (internal system clock; Fosc or 32768 Hz option by X12PA)

Notes : 1. The event counter behaves from low to high transition.

2. When the X12PA=0 and (TM0, TM1)=(1, 1), then the clock source is 32KHz.

3. When the X12PA=1 and (TM0, TM1)=(1, 1), then the clock source is the Fosc(4MHz).

4. X12PA is a configuration option by user (code layer option).

TS2	TS1	TS0	TMR Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

TMR1H, TMR1L (08h, 09h) & TMR1C (0Ah)

The TMR1 is a programmable 16-bit/8-bit count-up counter. The counter registers are named TMR1L (09h) and TMR1H (08h) respectively. The clock source is defined by the register of TMR1C. The TMR1C is its control register and the default value is 00. The definition of TMR1C is listed below.

Labels	Bits	Function
TON1	0	Timer1 enable/disable definition bit 0 = Disable; 1 = Enable
TS0, TS1, TS2	1 - 3	Timer clock source selection bits
—	4	Reserved, not used
TMROUT	5	The set the TMR as input or output pin. 0=input 1=output, it will generate a clock output from TMR pin.
TM0 TM1	6, 7	To define the operation mode 00= Timer mode (internal system clock; Fosc/4) 01= Timer mode (internal RC clock) 10= Event count mode (external clock) 11= Timer mode (internal system clock; Fosc or 32768 Hz option by X12PA)

- Notes :
1. The event counter behaves from low to high transition.
 2. When the X12PA=0 and (TM0, TM1)=(1, 1), the clock source is 32KHz.
 3. When the X12PA=1 and (TM0, TM1)=(1, 1), the clock source is the Fosc(4MHz).
 4. X12PA is a configuration option by user (code layer option).
 5. When the TMR pin is set as output, the initial state is low.

TMR2L (2bh) & TMR2C (2ch)

The TMR2 is a programmable 8-bit count-up counter. The clock source comes from Fosc/4, internal RC clock or external. The TMR2C is its control register and the default value is 00. The definition of TMR2C is listed below.

Labels	Bits	Function
TON2	0	Timer2 enable/disable definition bit 0 = Disable; 1 = Enable
TS0, TS1, TS2	1 - 3	Timer clock source selection bits
—	4	Reserved, not used
—	5	Reserved, not used
TM0 TM1	6, 7	To define the operation mode 00= Timer mode (internal system clock; Fosc/4) 01= Timer mode (internal RC clock) 10= Event count mode (external clock) 11= Timer mode (internal system clock; Fosc or 32768 Hz option by X12PA)

- Notes :
1. The event counter behaves from low to high transition.
 2. When the X12PA=0 and (TM0, TM1)=(1, 1), the clock source is 32KHz.
 3. When the X12PA=1 and (TM0, TM1)=(1, 1), the clock source is the Fosc(4MHz).
 4. X12PA is a configuration option by user (code layer option).

TMR3L (2dh) & TMR3C (2eh)

The TMR3 is a programmable 8-bit count-up counter. The clock source comes from Fosc/4, internal RC clock or external. The TMR3C is its control register and the default value is 00. The definition of TMR3C is listed below.

Labels	Bits	Function
TON3	0	Timer3 enable/disable definition bit 0 = Disable; 1 = Enable
TS0, TS1, TS2	1 - 3	Timer clock source selection bits
—	4	Reserved, not used
—	5	Reserved, not used
TM0 TM1	6, 7	To define the operation mode 00= Timer mode (internal system clock; Fosc/4) 01= Timer mode (internal RC clock) 10= Event count mode (external clock) 11= Timer mode (internal system clock; Fosc or 32768 Hz option by X12PA)

- Notes :
1. The event counter behaves from low to high transition.
 2. When the X12PA=0 and (TM0, TM1)=(1, 1), the clock source is 32KHz.
 3. When the X12PA=1 and (TM0, TM1)=(1, 1), the clock source is the Fosc(4MHz).
 4. X12PA is a configuration option by user (code layer option).

TS2	TS1	TS0	TMR Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

In timer mode, user should write an initial value to the counter registers (TMRnL, TMRnH) and then enable the TONn (TMRnC.0). The TMRn will count-up with the rate of TS0 – TS2 & TM0, TM1 setting. When timer is overflow (ffffh --> 0000h), system will generate an interrupt and the corresponding flag will be set to "1", if both the global interrupt bit and the corresponding bit are enabled. After timer is overflow, the initial value will reload to counter register automatically unless the TMRn is disabled.

In event count mode, counter registers will count up a step when the TMR pin inputs a changing state from "L" to "H". When the timer is overflow and the corresponding control bits are set, the system will also generate an interrupt.

Data Access (1Eh, 1Fh)

For the JA23048 & JA23060, data is accessed by index addressing instruction. so the CROMRCONT (1Eh) and CROMADD (1Fh) registers are useless.

For the JA23384~JA231K0 bodies, data is accessed by CROMCONT & CROMADD to addressing and read data.

Watchdog Timer

WDTCLR (W)

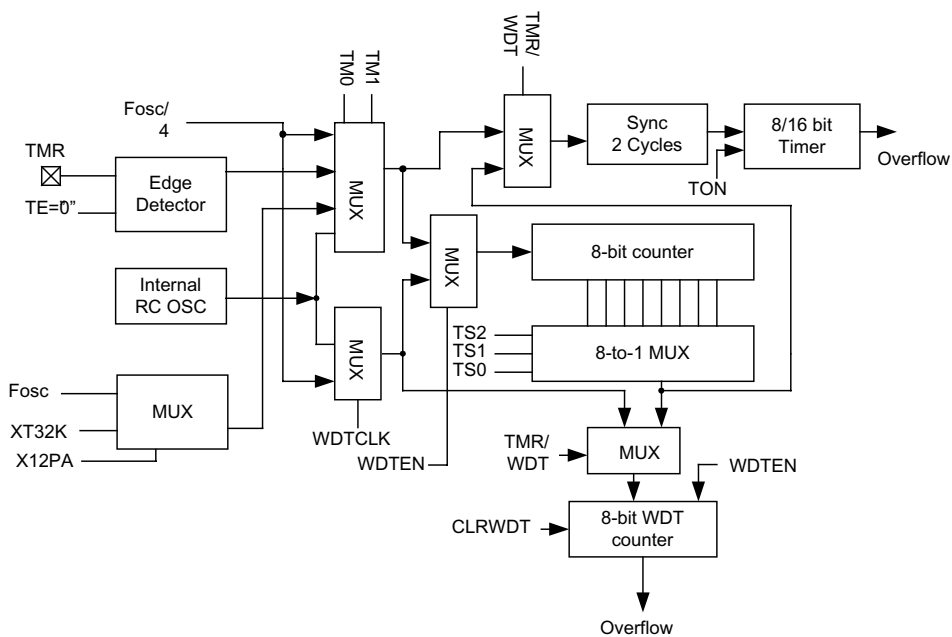
Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03h	—	—	—	—	—	—	—	CLRWDT

Bit 0 (CLRWDT) : To prevent a WDT time-out, reset is done by writing a “1” to this bit within a specific time WDTCL (R/W)

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04h	—	—	—	WDTCLK	—	—	—	WDTEN

Bit 4 (WDTCLK) : To select the WDT clock source
 0=Fosc/4 (Default), 1= Internal RC clock

Bit 0 (WDTEN) : To enable/disable the WDT
 0= Disable (Default), 1= Enable



Interrupt

Interrupt request is generated by IRQ bar and will keep 9 ~ 16 cycles. If commands between “SEI” and “CLI” are over 9 instruction cycles, the interrupt may be lost but corresponding interrupt bit (INTF.X) will still be set (“1”). User can check INTF to avoid loss of interrupt.

When an interrupt is generated, the interrupt vector (\$FFFE, \$FFFF) will be loaded to PCL and PCH (PCL, PCH: Program Counter) and the original data in PCL, PCH & Status register content will be saved in stack. The corresponding interrupt bit (INTF.X) will be set (Write in “1”) Automatically. After the instruction of “RTI” is executed, the original data will be pulled out from stack and saved to original registers. When the interrupt program is executed, the corresponding bit of interrupt flag (INTF.X) should be cleared (Write in “0”) by user program.

The interrupt source include one of the following conditions :

- Timer overflow
- PA, PB, PC change state input
- External interrupt input

INTC (R/W)

Register	Bit No.	Label	Function
INTC	0	INTE	Global interrupt enable bit (1= Enabled; 0 = Disabled)
	1	INT	External INT pin interrupt Enable bit (1= Enabled; 0 = Disabled)
	2	TMR0	TMR0 interrupt Enable bit (1= Enabled; 0 = Disabled)
	3	TMR1	TMR1 interrupt Enable bit (1= Enabled; 0 = Disabled)
	4	PAI	Port A change state interrupt Enable bit (1= Enabled; 0 = Disabled)
	5	PBI	Port B change state interrupt Enable bit (1= Enabled; 0 = Disabled)
	6	PCI/1ms	Port C or 1ms change state interrupt Enable bit (1= Enabled; 0 = Disabled)
	7	TMR2/TMR3	TMR2 or TMR3 interrupt Enable bit (1= Enabled; 0 = Disabled)

INTF (R/W)

Register	Bit No.	Label	Function
INTF	0	INTF	External INT interrupt flag bit (1= Active; 0 = Inactive)
	1	TMR0F	TMR0 timer interrupt flag bit (1= Active; 0 = Inactive)
	2	TMR1F	TMR1 timer interrupt flag bit (1= Active; 0 = Inactive)
	3	TMR2F	TMR2 timer interrupt flag bit (1= Active; 0 = Inactive)
	4	PAF	Port A change state interrupt flag bit (1= Active; 0 = Inactive)
	5	PBF	Port B change state interrupt flag bit (1= Active; 0 = Inactive)
	6	PCF/1ms	Port C or 1ms change state interrupt flag bit (1= Active; 0 = Inactive)
	7	TMR3F	TMR2 or TMR3 timer interrupt flag bit (1= Active; 0 = Inactive)

Note : 1. The time period of 1ms is generated when the system frequency is 2MHz.

2. The INTF can write-in “0” only. The data of “1” is ineffective. If user wants to clear INTF, don’t use the command “AND”, must write-in “0” to INTF immediately, see the Example for INTF process.

3. After the interrupt program is executed, the corresponding flag should be cleared by software.

4. If using port change-state interrupt, be sure to read port state before returning from interrupt subroutine. Without reading port state again, system might be unstable.

Example for INTF process

INTREQUEST:

```
sei
pha
txa
pha
lda INTF          ;check TMR0 interrupt
bit  #$02
beq  OtherINT
jsr  TMR0_interrupt
```

OtherINT:

```
...
pla
tax
pla
cli
rti
```

TMR0_interrupt:

```
lda  #$FD          ;clear TMR0 interrupt flag;INTF only write "0"
sta  INTF
...
rts
```

Wake up

The wake-up source include one of the following condition :

- Timer overflow
- PA, PB, PC change state input
- External interrupt input

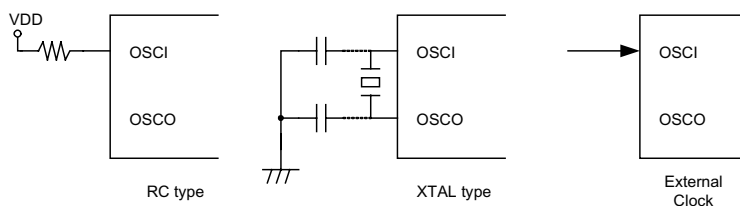
When the global interrupt bit (INTE) is disabled and the corresponding I/O port (PA, PB & PC) interrupt bit is enabled, the wakeup source will generate wakeup without interrupt.

After the interrupt is generated, the system will be activated from HALT mode or the STOP mode and then the program counter will increase and the next instruction will be executed continuously. All of the content of registers will be unchanged.

Oscillator

The JA23000 SERIES supports three types of oscillation circuit; they are RC, XTAL1 (High frequency) and XTAL2 (low frequency). For the RC type, an external resistor connection between OSC1 and VDD. For the crystal/resonator type, one of the crystal or resonator is connected to OSC1 and OSC0. For the crystal mode, it can be optioned as high frequency and low frequency operating mode.

For the XTAL mode, the system will delay 1024 clocks after power is turned on or the system is waken-up from the stop mode. And for the RC mode, the system will delay 64 clocks.



Reset

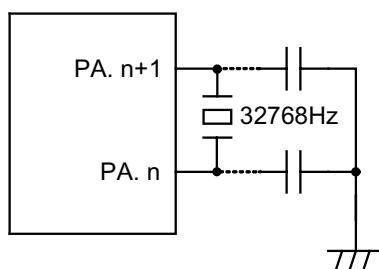
There are 5 conditions will reset the system

- Power on reset
- Reset pin active
- Illegal address generation
- WDT overflow
- VDD voltage lower than 1.8V

When the system is reset, the reset vector (\$FFFC, \$FFFD) will load to PCL, PCH and the instruction in the vector will be executed immediately. Only the power-on reset (cold reset) can initialize the internal register, the others reset (warm reset) can't change the content of all registers.

PA & 32768 generator

The PA port can share 2 pins to generate 32K frequency for internal timer by mask option. For various bodies, the pins of 32K generator would be different.



Mask Option

- a. TMR0 & TMR1 length: (16-bit or 8-bit)
- b. AUD1, AUD2 output: (DAC, PWM)
- c. PC pull high: (With, Without)
- d. PA pin option: (I/O, 32K oscillator)
- e. PC/1mS interrupt source : (PC port, 1mS)

Register Initial Summarized

Register	Address	Power on reset	Reset (WDT Overflow, RESB Active, Illegal address)	Reset (WDT overflow from Halt)
INTC	01h	0000 0000	0000 0000	uuuu uuuu
INTF	02h	0000 0000	0000 0000	uuuu uuuu
WDTCLR	03h	-----	-----	uuuu uuuu
WDTC	04h	--- 0 --- 0	--- 0 --- 0	uuuu uuuu
TMRH	05h/08h	uuuu uuuu	uuuu uuuu	uuuu uuuu
TMRL	06h/09h	uuuu uuuu	uuuu uuuu	uuuu uuuu
TMRC	07h/0Ah	0000 0000	0000 0000	uuuu uuuu
PA, PB, PC	0Bh/0Eh/11h	1111 1111	1111 1111	uuuu uuuu
PAC, PBC, PCC	0Ch/0Fh/1Dh	1111 1111	1111 1111	uuuu uuuu

Absolute Maximum Rating

Symbol	Rating	Unit
$V_{DD} \sim V_{SS}$	-0.5 ~ +0.5	V
VIN (for input)	$V_{SS} - 0.3 < V_{IN} < V_{DD} + 0.3$	V
VOUT (for all outputs)	$V_{SS} < V_{OUT} < V_{DD}$	V
T (operating)	-10 ~ +60	°C
T (storage)	-55 ~ +125	°C

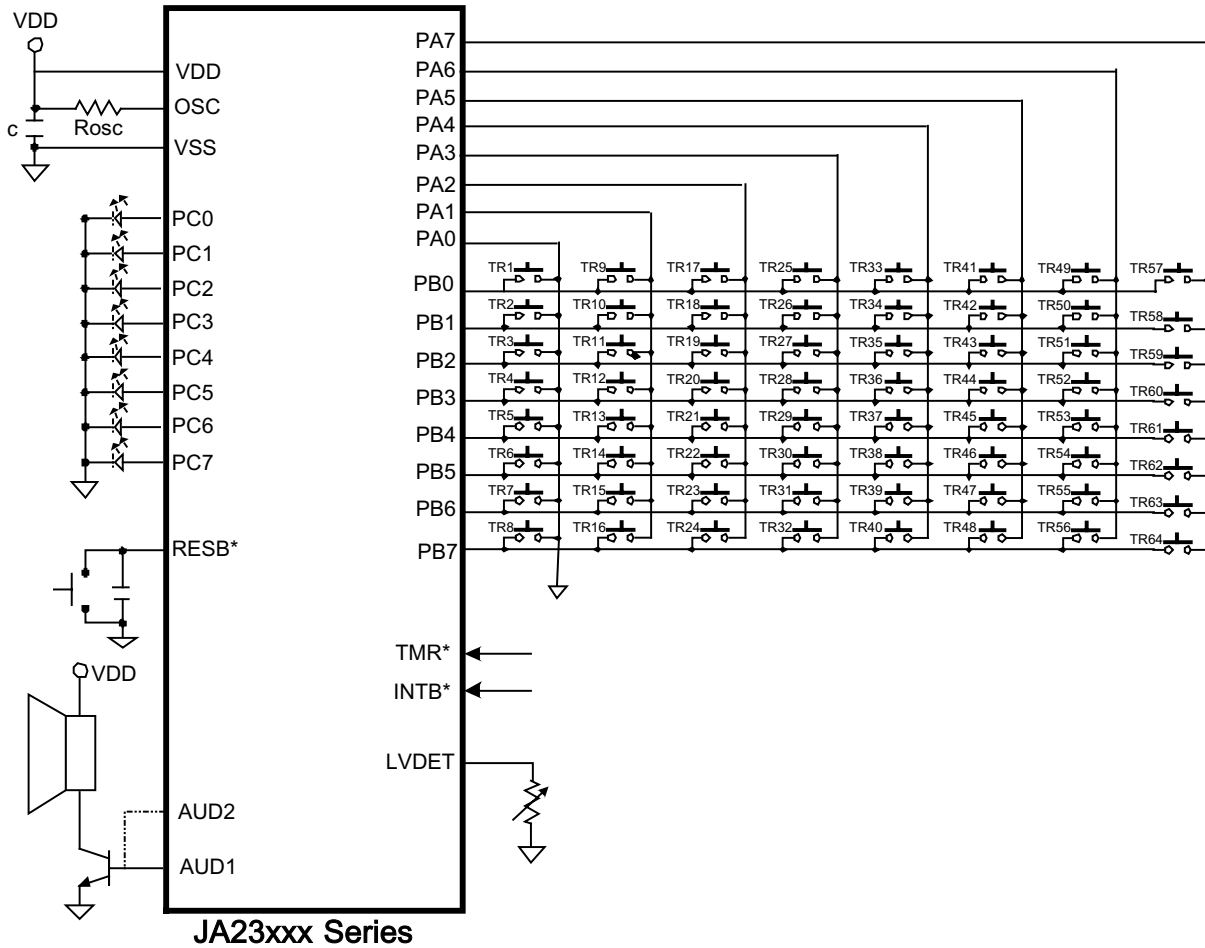
Electrical Characteristics
D.C. Characteristics

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		VDD	Condition				
VDD	Operating Voltage	—	—	2.4	—	5.2	V
IDD1	Operating Current (Crystal OSC)	3.3V	Fsys=4MHz	—	1	2	mA
IDD2	Operating Current (RC OSC)	3.3V	Fsys=4MHz	—	1	2	mA
ISTB1	Standby Current (Internal RC ON)	3.3V	No Load, System HALT	—	5	10	μA
ISTB2	Standby Current (Internal RC OFF)	3.3V	No Load, System HALT, Voltage Detector OFF	—	1	2	μA
VIL1	Input Low Voltage for I/O, TMR and INTB	3.3V	—	0	—	0.3VDD	V
VIH1	Input High Voltage for I/O, TMR and INTB	3.3V	—	0.7VDD	—	VDD	V
VIL2	Input Low Voltage for RESB	3.3V	—	0	—	0.4VDD	V
VIH2	Input High Voltage for RESB	3.3V	—	0.8VDD	—	VDD	V
VRES	Power reset voltage	—	VDD ≤ VRES, System re-start	1.6	1.8	2.0	V
IOL	I/O Sink Current	3.3V	VOL=0.1VDD	4	8	—	mA
IOH	I/O source Current	3.3V	VOH=0.9VDD	-2	-4	—	mA
RPH	Pull-High Resistance	3.3V	VIL=0V	50	100	150	kΩ

A.C. Characteristics

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		VDD	Condition				
FSYS1	System Clock (High Frequency Crystal OSC)	3.3V	—	400	—	4000	kHz
FSYS2	System Clock (RC OSC)	3.3V	—	400	—	6000	kHz
fTMR	TMR Input Frequency	3.3V	—	0	—	4000	kHz
tIRCO	Internal RC Oscillator period	3.3V	(About 32kHz)	66	33	22	μS
TWDT1	Watchdog Time-out Period (RC)	3.3V	Without pre-scaler (33 * 256)	16	8	5	mS
TWDT2	Watchdog Time-out Period (System clock)	3.3V	Without pre-scaler (4/Fsys * 256)	—	1024	—	tSYS
tRES	External Reset Low pulse Width	—	—	1	—	—	μS
TSST1	System Start-up Timer Period	—	Power-up, reset or wake-up from Halt (Crystal OSC)	—	1024	—	tSYS
TSST2	System Start-up Timer Period	—	Power-up, reset or wake-up from Halt (RC OSC)	—	64	—	tSYS
tRES	Interrupt pulse Width	—	—	1	—	—	μS

Application Circuit



- Note :
1. The IC substrate should be connect to VSS
 2. The RESB, INTB, &TMR should be connect to VDD, if don't use.