

2-Channel Dual Slope ADC with Regulator

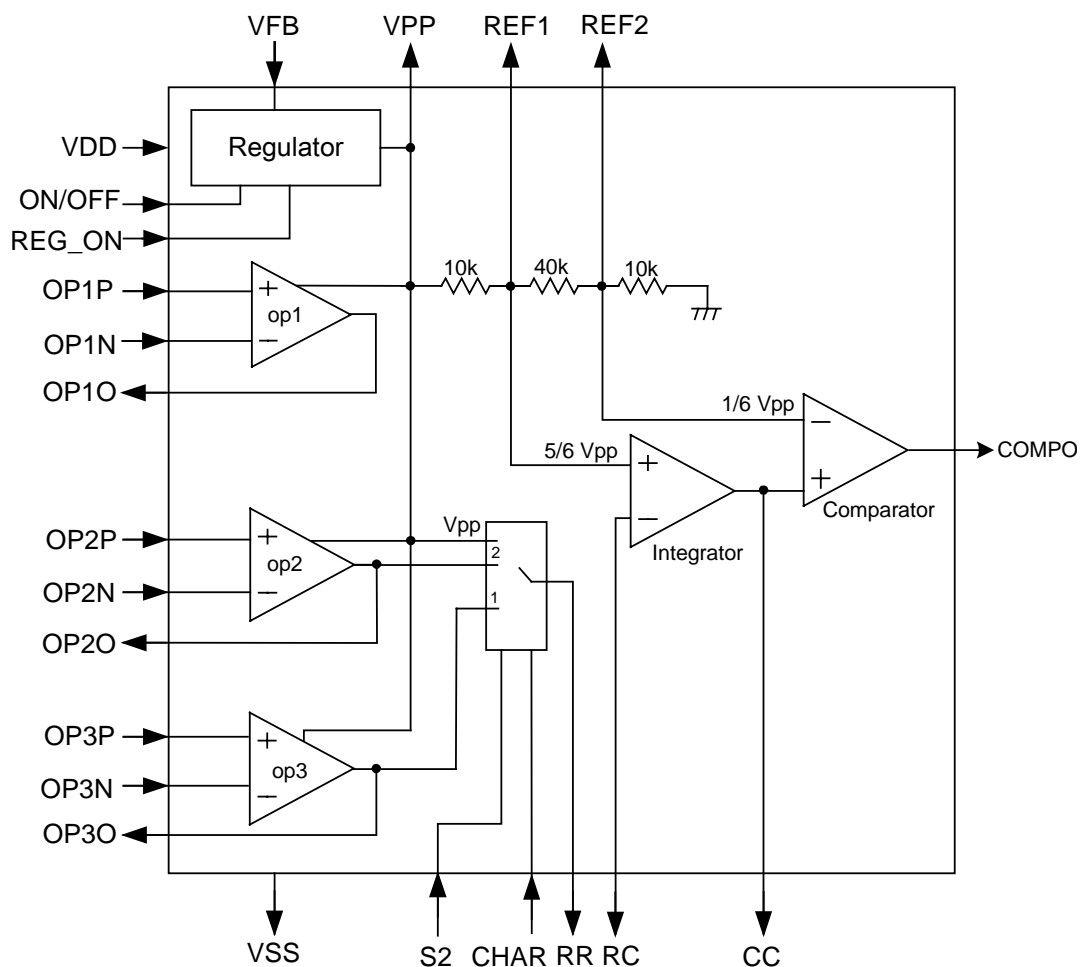
Feature

- Operating Voltage: 2.4 V ~ 5.2 V
- Operation Current: 300 μ A @ VDD=3V
- Standby current: 0.1 μ A @ VDD=3V
- Regulator source current: 20 mA @ VDD=3V
- Three Operation Amplifiers with channel switch suitable for 2-channel application
- Integrator and Comparator for dual slope function
- ON/OFF pin for chip enable/disable control
- REG_ON pin for regulator enable/disable control

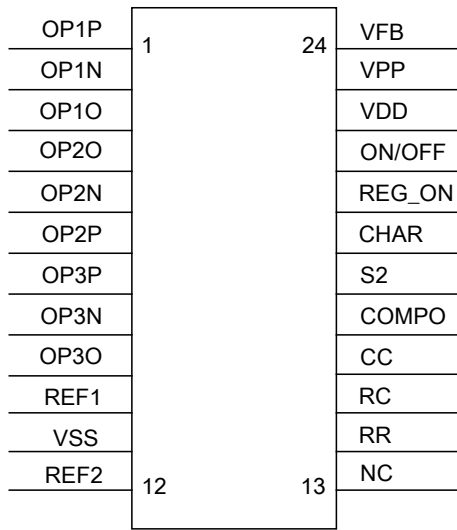
General Description

The JA32030 offers two-channel A/D conversion at low cost by using Dual Slope integration structure. It incorporates regulator, operational amplifiers, integrator, comparator and control circuit inside to achieve high performance for measuring application.

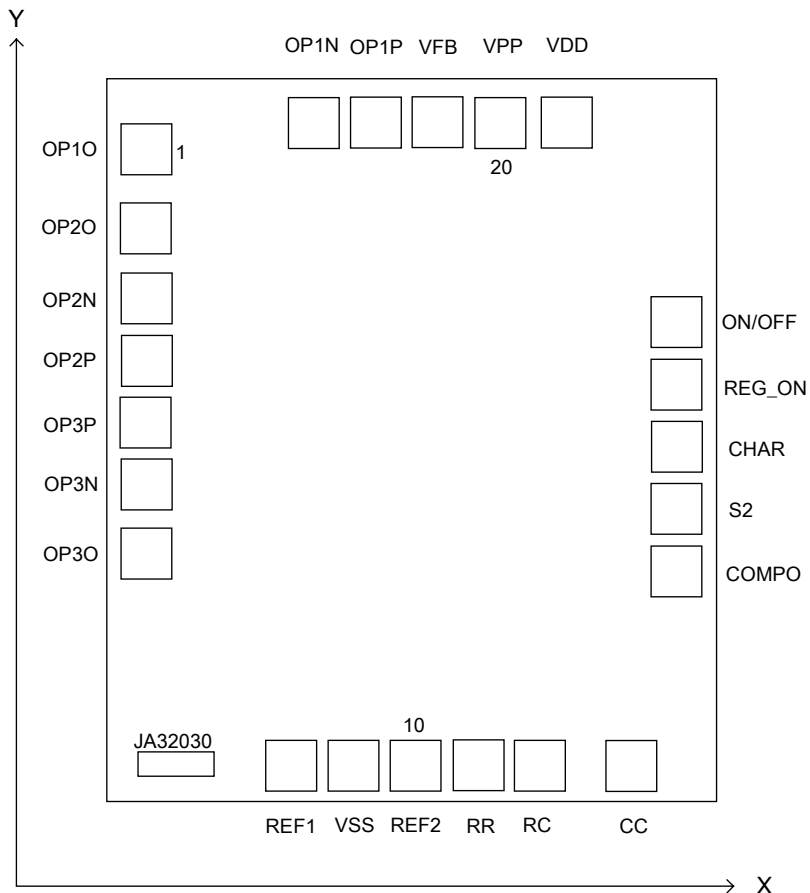
Block Diagram



Pin Assignment



Pad Assignment



Pad Coordinates

Pad No.	Pad Name	X (μm)	Y (μm)
1	OP1O	70	1162.2
2	OP2O	70	1021.4
3	OP2N	70	898.3
4	OP2P	70	788.1
5	OP3P	70	677.9
6	OP3N	70	567.7
7	OP3O	70	445.6
8	REF1	327.2	70
9	VSS	437.4	70
10	REF2	547.6	70
11	RR	657.8	70
12	RC	768	70
13	CC	930.1	70
14	COMPO	1010	415.1
15	S2	1010	525.3
16	CHAR	1010	635.5
17	REG-ON	1010	745.7
18	ON/OFF	1010	855.9
19	VDD	815.3	1210
20	VPP	697.1	1210
21	VFB	586.9	1210
22	OP1P	476.7	1210
23	OP1N	366.5	1210

Pad Description

Pin No	Pad No	Pad Name	I/O	Description
1	22	OP1P	I	OP1 "+" input terminal
2	23	OP1N	I	OP1 "-" input terminal
3	1	OP1O	O	OP1 output terminal
4	2	OP2O	O	OP2 output terminal
5	3	OP2N	I	OP2 "-" input terminal
6	4	OP2P	I	OP2 "+" input terminal
7	5	OP3P	I	OP3 "+" input terminal
8	6	OP3N	I	OP3 "-" input terminal
9	7	OP3O	O	OP3 output terminal
10	8	REF1	O	5/6 VPP reference voltage
11	9	VSS	O	GND
12	10	REF2	O	1/6 VPP reference voltage
13		NC		Not used
14	11	RR	O	Charge and discharge source
15	12	RC	I	Integrator "-" input terminal
16	13	CC	O	Integrator output terminal
17	14	COMPO	O	Comparator output terminal
18	15	S2	I	Channel select control; without internal pull high
19	16	CHAR	I	1: charge, 0: discharge; without internal pull high

20	17	REG_ON	I	Regulator on/off control; without internal pull high
21	18	ON/OFF	I	1: ADC circuit on; without internal pull high 0: ADC circuit off
22	19	VDD	I	Power input
23	20	VPP	O	Regulator output
24	21	VFB	I	Regulator reference voltage input terminal, 1.25V

Electrical Characteristics

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		VDD	Condition				
VDD	Operation Voltage			2.4	3.0	5.2	V
IDD	Operation Current	3V	With Loading	-	300	500	μA
ISTB	Standby Current	3V	ON/OFFpin:0	-	0.1	1	μA

Functional Descriptions

1. ON/OFF

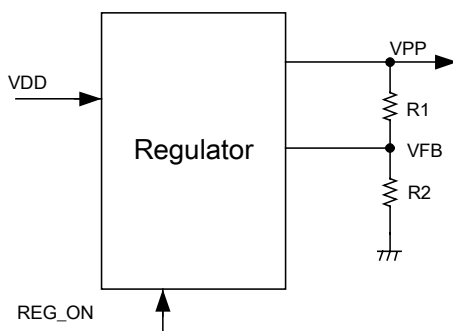
This signal is used to enable or disable JA32030. The “1” level on this pin activate the JA32030, “0” level put the chip in stop mode for power saving. The VPP won’t be available unless the ON/OFF is active (High).

2. Regulator

The regulator can output either regulated or unregulated VPP for internal ADC (analog-digital conversion) circuit. The VPP can be either regulated or unregulated (same as VDD) controlled by REG_ON status. Please refer to the table below.

	1	0
REG_ON	Regulator on	Regulator off, VPP = VDD

The VPP can be decided by R1. The VFB voltage shall be always 1.25V.



$$VPP = (1.25 \text{ V} / R2) \times (R1 + R2)$$

3. OP1, OP2 and OP3

OP1 is a low noise amplifier especially designed for first level signal amplification. It is a PMOS two-stage amplifier structure. OP2 and OP3 were designed for second level signal amplification. Both OP2 and OP3 are NMOS two-stage amplifier structure.

These three OP amplifiers are independent to each other; users can choose the proper OP combination for their own application.

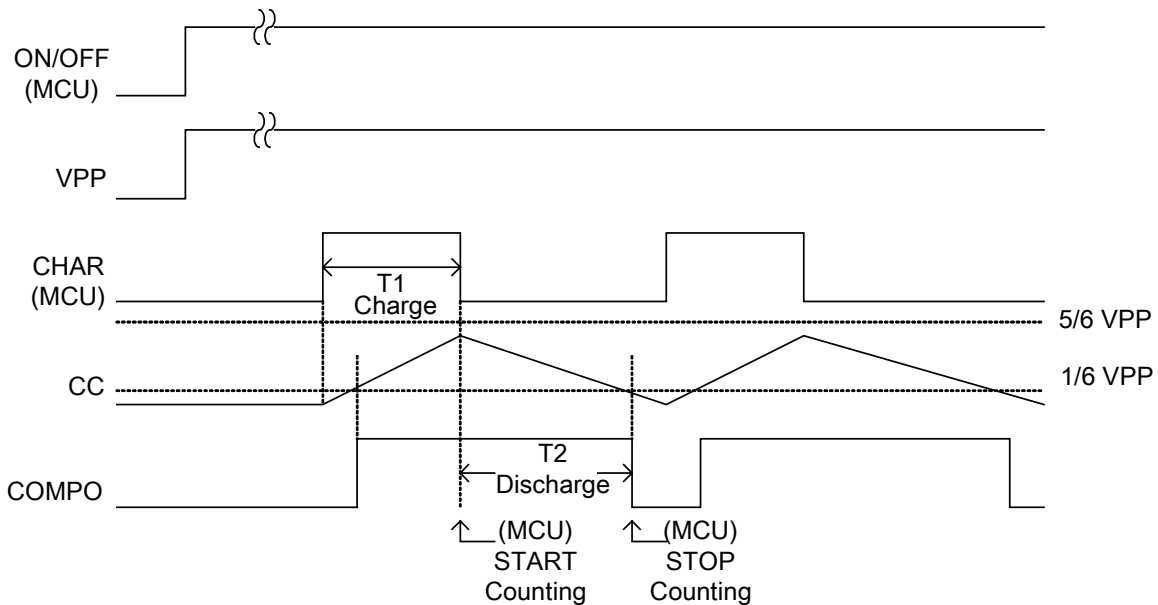
4. Channel switching:

To provide a flexible application field, the JA32030 embedded an analog switch to fulfill the two-channel application. The control signal S2 decides the channel selection.

S2	1	0
Channel Input	OP2 selected	OP3 selected

5. Comparator

The comparator is used to generate a data to controller. When the input signal is charged on integrator after a time interval T1, the controller shall control the CHAR pin to discharge (See the Timing Diagram), and then controller shall enable the internal counter to start counting. When the voltage on CC is lower than 1/6 VDD (after discharge a time interval T2), the COMPO pin will transfer from High to Low. At this time the controller shall stop the internal counter. The discharge time T2 is proportional to the input level, the final count of counter can be converted to digital data by controller.

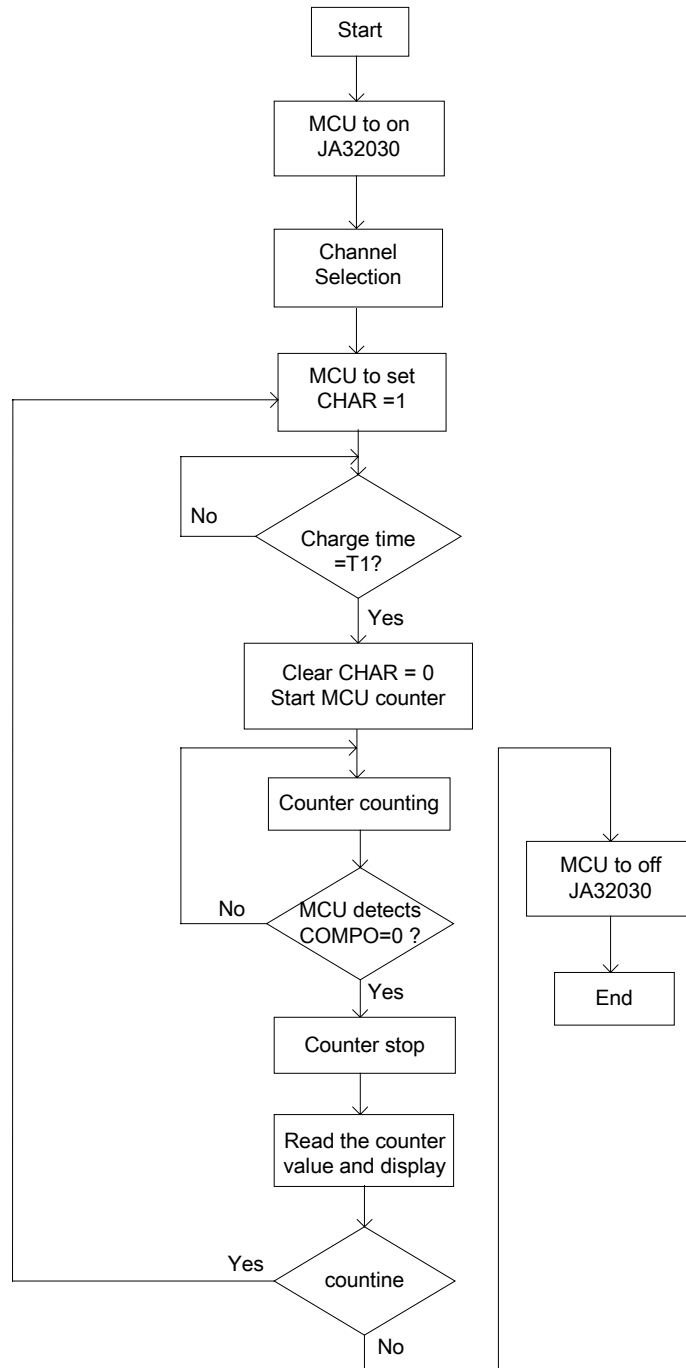
Timing Diagram


T1(Charge): The fixed charge time control by controller(MCU).

T2 (Discharge): The discharge time provide to controller(MCU).

Programming Flow Chart

The following flow chart is the illustration for JA32030 programming.



- a. MCU asserts high signal on JA32030 ON/OFF pin to activate JA32030.
- b. JA32030 provides power to sensor from SPWR pin.
- c. MCU asserts high signal on JA32030 CHAR pin to inform JA32030 start charging.

- d. After a fixed time interval (decided by MCU program), MCU asserts low signal on JA32030 CHAR pin to inform JA32030 start discharging.
- e. MCU enable internal counter start counting.
- f. When ADCC of JA32030 below 1/6 VDD (The COMPO pin transfer from High to Low), MCU disable counter.
- g. MCU converts counter count value to digital output. The count value is proportional to the input signal.

Application Diagram

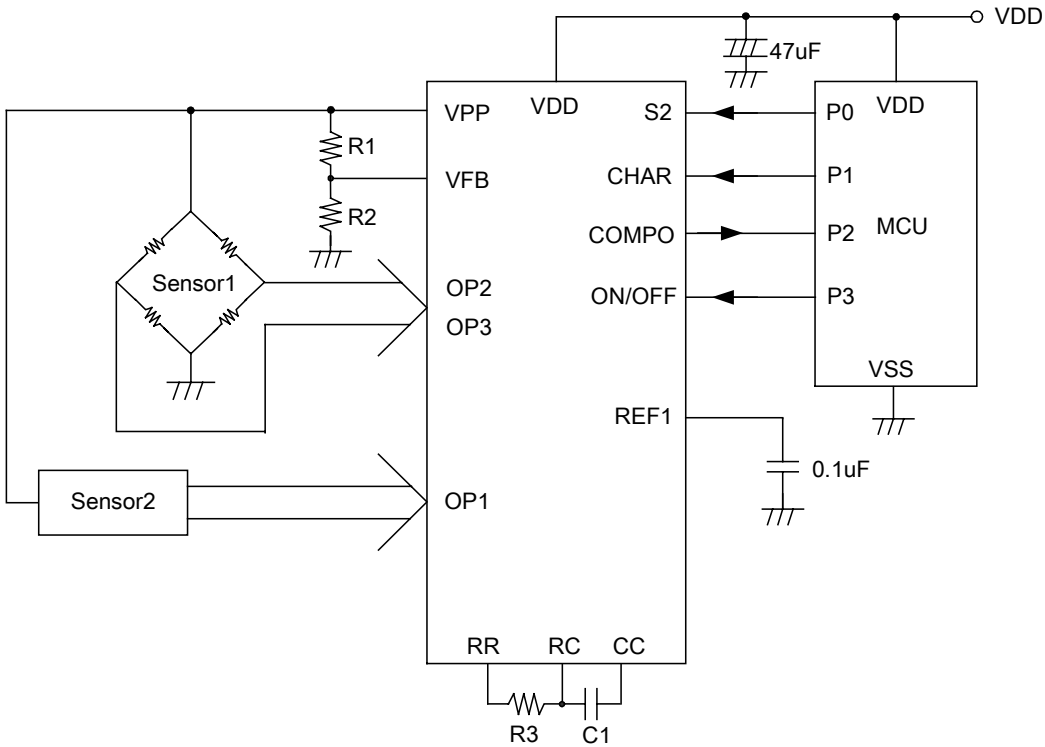


Table1. 充電時間 104mS 比較表

R	C	T1 (充電時間)	T2 (放電時間)
300K	0.1uF	104mS	142mS
500K	0.1uF	104mS	140mS
680K	0.1uF	104mS	140mS
820K	0.1uF	104mS	136mS

Table2. 充電時間 80mS 比較表

R	C	T1 (充電時間)	T2 (放電時間)
300K	0.1uF	80mS	98mS
500K	0.1uF	80mS	90mS

680K	0.1uF	80mS	84mS
820K	0.1uF	80mS	82mS

Table3. 充電時間 64mS 比較表

R	C	T1 (充電時間)	T2 (放電時間)
300K	0.1uF	64mS	66mS
500K	0.1uF	64mS	56mS
680K	0.1uF	64mS	50mS
820K	0.1uF	64mS	48mS

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