Features

- Low power dissipation
- Powerful instruction set (148 instructions)
  - Binary addition, subtraction, BCD adjustment, logical operation, direct addressing mode and index addressing mode
  - Single-bit manipulation (Set, Reset, Conditional branch)
  - Various conditional branches
  - 16 working registers and manipulation
  - LCD driver with data transfer
  - Look-up table
  - Programmable peripheral option
  - System clock selection
- Memory capacity
  - Instruction ROM capacity 2048 x 16 bits
  - Index ROM capacity 256 x 8 bits
  - Internal RAM capacity 256 x 4 bits (low-address 128 nibbles can be accessed by direct addressing, full-range 256 nibbles can be accessed by index addressing)
- Input/output ports
  - Port IOA 4 pins (with internal pull-low, chattering clock, MUX with CX, RR, RT, RH and SEG 37~40 by mask option)
  - Port IOB 4 pins (MUX with ELC, ELP, BZB, BZ and SEG41, 42 by mask option)
  - Port IOC 4 pins (with internal pull-low, low-level hold, chattering clock, MUX with AN1~4 by mask option)
  - Port IOD 4 pins (MUX with PWM1, 2 and SEG33~36 by mask option)
- 8-level subroutine nesting
- Dual clock operation
- Interrupt function
  - External factor 2 (INT pin & port IOA, IOC input)
  - Internal factor 4 (pre-divider, 2 timers & RFC)
- Built-in EL-light driver, alarm, frequency or melody generator
- Built-in R to F converter circuit
- Built-in comparator, 2 sets of 6/8-bit PWM output, 4-bit D/A converter, this structure can be used as a 4/6/8-bit full range 4ch ADC
- 2 sets of 6-bit programmable timers with programmable clock source
- Watchdog timer
- LCD/LED driver output
  - 4 * 42 LCD/LED driver outputs (Up to 168 LCD segments are drivable)
  - Mask option is used to select static, 1/2 bias 1/2 duty, 1/2 bias 1/3 duty, 1/2 bias 1/4 duty, 1/3 bias 1/3 duty and 1/3 bias 1/4 duty drive modes of the LCD panel
  - Mask option is used to select DC output, and static, 1/2 duty, 1/3 duty and 1/4 duty drive modes of the LED panel
  - Mask option is used to select SEG1~32 as P open-drain or CMOS outputs
  - Single instruction stops all segments that are either in LCD or LED
- Built-in voltage Doubler, Halver, Tripler charge pump circuit
- HALT function
- Stop function

Notice :The JA54270 chip's LBR function was cancelled since 2004/11/11.

General Description

JA54270 is an embedded high-performance 4-bit microcomputer with an LCD/LED driver. It contains all the necessary functions in a single chip:
4-bit parallel processing ALU, ROM, RAM, I/O ports, timer, clock generator, dual clock, ADC, RFC, alarm, EL-light, LCD driver, look-up table and watchdog timer. The instruction set consists of 148 instructions that include nibble operation, manipulation, various conditional branch instructions and LCD data transfer instructions which are powerful and easy to follow.

The HALT function stops any internal operations other than the oscillator, divider and LCD driver in order to minimize the power dissipation.

The stop function stops all clocks in the chip.

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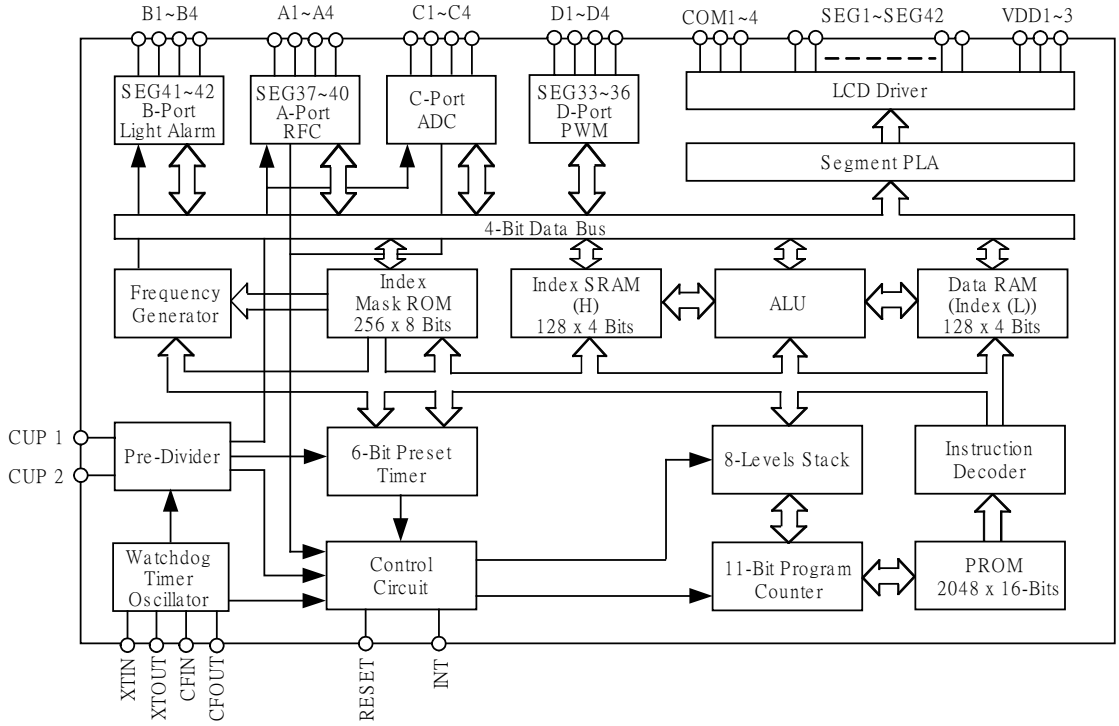
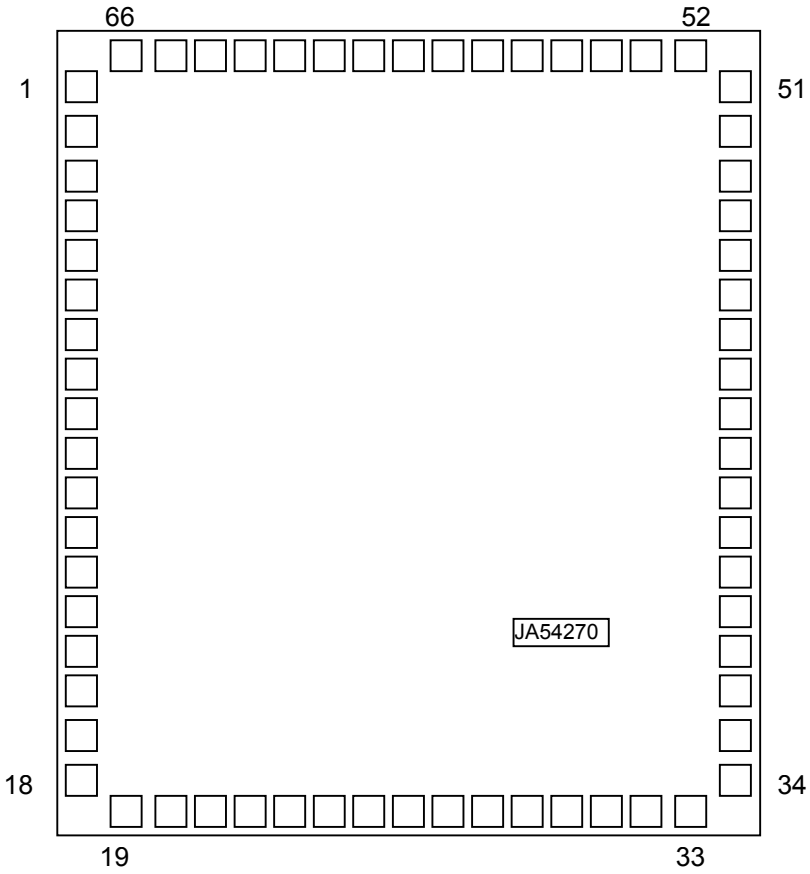
Block Diagram



Pad Assignment



The substrate must connect to GND.

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Pad Coordinates

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	BAK	70	2175	34	SEG13	1970	160
2	CFIN	70	2045	35	SEG14	1970	290
3	CFOUT	70	1915	36	SEG15	1970	420
4	XTIN	70	1800	37	SEG16	1970	535
5	XTOUT	70	1685	38	SEG17	1970	650
6	TESTA	70	1570	39	SEG18	1970	765
7	RESET	70	1455	40	SEG19	1970	880
8	INT	70	1340	41	SEG20	1970	995
9	IOC1/AN1	70	1225	42	SEG21	1970	1110
10	IOC2/AN2	70	1110	43	SEG22	1970	1225
11	IOC3/AN3	70	995	44	SEG23	1970	1340
12	IOC4/AN4	70	880	45	SEG24	1970	1455
13	VDD1	70	765	46	SEG25	1970	1570
14	VDD2	70	650	47	SEG26	1970	1685
15	VDD3	70	535	48	SEG27	1970	1800
16	CUP1	70	420	49	SEG28	1970	1915
17	CUP2	70	290	50	SEG29	1970	2045
18	COM1	70	160	51	SEG30	1970	2175
19	COM2	200	70	52	SEG31	1840	2265
20	COM3	330	70	53	SEG32	1710	2265
21	COM4	445	70	54	SEG33/IOD1	1595	2265
22	SEG1	560	70	55	SEG34/IOD2	1480	2265
23	SEG2	675	70	56	SEG35/IOD3/PWM1	1365	2265
24	SEG3	790	70	57	SEG36/IOD4/PWM2	1250	2265
25	SEG4	905	70	58	SEG37/IOA1/CX	1135	2265
26	SEG5	1020	70	59	SEG38/IOA2/RR	1020	2265
27	SEG6	1135	70	60	SEG39/IOA3/RT	905	2265
28	SEG7	1250	70	61	SEG40/IOA4/RH	790	2265
29	SEG8	1365	70	62	SEG41/IOB1/ELC	675	2265
30	SEG9	1480	70	63	SEG42/IOB2/ELP	560	2265
31	SEG10	1595	70	64	IOB3/BZB	445	2265
32	SEG11	1710	70	65	IOB4/BZ	330	2265
33	SEG12	1840	70	66	GND	200	2265
Chip size: 2040 x 2335um / Pad Open: 90 x 90um / Pad Pitch: 115um							

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Pad Descriptions

Pad Name	I/O	Description
VDD		Positive back-up voltage. In Li mode, connects a 0.1u capacitance to GND.
VDD1 VDD2 VDD3		LCD drives the voltage and positive supply voltage. While in Ag mode, connects +1.5V to VDD1. While in Li / EXT-V mode, connects +3.0V to VDD2.
RESET	I	Input pin from LSI reset request signal. Built in pull-down resistor.
INT	I	Input pin for external INT request signal. Falling or rising edge triggered by mask option. Internal pull-down or pull-up resistor or none is selected by mask option.
TESTA	I	Test signal input pin. Built in pull-down resistor.
CUP1 CUP2	O O	Switching pins for supplying the LCD driving voltage to the VDD1, 2, 3 pins. Connects the CUP1 and CUP2 pins with no polarized electrolytic capacitor if 1/2 or 1/3 bias mode has been selected. In the static mode, these pins should be open.
XTIN XTOUT	I O	Time-based counter frequency (clock-specified, LCD alternating frequency , Alarm signal frequency) or system clock oscillation. 32kHz crystal oscillator. Oscillation stops at the execution of STOP instruction.
CFIN CFOUT	I O	System clock oscillation. Connected with ceramic resonator. Connected with RC oscillation circuit. Oscillation stops at the execution of STOP or SLOW instruction.
COM1~4	O	Output pins for supplying voltage to drive the common pins of the LCD or LED panel.
SEG1~42	O	Output pins for LCD or LED panel segment.
IOA1~4	I/O	Input/Output port A can use software to define the internal pull-low resistor And chattering clock in order to reduce input bounce and generate interrupt. This port shares pins with SEG37~40 and is set by mask option. This port also shares pins with CC, RR, RT and RH, and is set by mask option.
IOB1~4	I/O	I/O Input/Output port B. IOB1, 2 shares pins with SEG41, 42, or ELC, ELP and is set by mask option. IOB3, 4 shares pins with BZ, BZB and is set by mask option.
IOC1~4	I/O	I/O Input/Output port C can use software to define the internal pull-low / Low-level hold resistor and chattering clock in order to reduce input bounce And generate interrupt. This port shares pins with AN1-4 and is set by Mask option.
IOD1~4	I/O	Input / Output port D. This port shares pins with SEG33~36 and is set by mask option. IOD3, 4 shares pins with PWM1, 2 and is set by mask option.
CX RR RT RH	I O O O	1 input pin and 3 output pins for RFC application. This port shares pins with SEG37~40 and is set by mask option. This port shares pins with IOA1~4 and is set by mask option.
ELC ELP	O O	Output port for the EL-light. These ports share pins with SEG41, 42 and are set by mask option. These ports share pins with IOB1, 2 and are set by mask option.
BZB BZ	O O	Output port for alarm, frequency or melody generator. This port shares pins with IOB3, 4 and is set by mask option.

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Pad Name	I/O	Description
GND		Negative supply voltage.

Absolute Maximum Rating

Ta = 0 to 70℃ GND=0V

Name	Symbol	Rating	Unit
Maximum Supply Voltage	V_{DD1}	-0.3 ~ +4.4	V
	V_{DD2}	-0.3 ~ +4.4	V
	V_{DD3}	-0.3 ~ +6.6	V
Maximum Input Voltage	V_{IN}	-0.3 to $V_{DD1/2}$+0.3	V
Maximum Output Voltage	V_{OUT1}	-0.3 to $V_{DD1/2}$+0.3	V
	V_{OUT2}	-0.3 to V_{DD3}+0.3	V
Maximum Operating Temperature	t_{OPG}	0 to +70	℃
Maximum Storage Temperature	t_{STG}	-25 to +125	℃

Allowable operating conditions

Ta = 0 to 70℃ GND=0V

Name	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	V_{DD1}		1.2	4.2	V
	V_{DD2}		2.2	4.2	V
	V_{DD3}		2.2	6.3	V
Supply Voltage	V_{DD1}	Ag Mode	1.2	1.7	V
	V_{DD2}	EXT-V, Li Mode	2.2	4.2	V
Oscillator Start-up Supply Voltage	V_{DD1}	Crystal; Ag Mode	1.2	-	V
	V_{DD2}	Crystal; EXT-V, Li Mode	2.4	-	
Oscillator Sustain Supply Voltage	V_{DD1}	Crystal; Ag Mode	1.2	-	V
	V_{DD2}	Crystal; EXT-V, Li Mode	2.2	-	
Input ″H″ Voltage	V_{IH1}	Ag Battery Mode	$V_{DD1-0.7}$	$V_{DD1+0.7}$	V
Input ″L″ Voltage	V_{IL1}		-0.7	0.7	V
Input ″H″ Voltage	V_{IH2}	Li Battery Mode	$V_{DD2-0.7}$	$V_{DD2+0.7}$	V
Input ″L″ Voltage	V_{IL2}		-0.7	0.7	V
Input ″H″ Voltage	V_{IH3}	OSCIN at Ag Battery Mode	$0.8V_{DD1}$	V_{DD1}	V
Input ″L″ Voltage	V_{IL3}		0	$0.2V_{DD1}$	V
Input ″H″ Voltage	V_{IH4}	OSCIN at Li Battery Mode	$0.8V_{DD2}$	V_{DD2}	V
Input ″L″ Voltage	V_{IL4}		0	$0.2V_{DD2}$	V
Input ″H″ Voltage	V_{IH5}	CFIN at Li Battery or EXT-V Mode	$0.8V_{DD2}$	V_{DD2}	V
Input ″L″ Voltage	V_{IL5}		0	$0.2V_{DD2}$	V
Input ″H″ Voltage	V_{IH6}	RC Mode	$0.8V_{DDO}$	V_{DDO}	V
Input ″L″ Voltage	V_{IL6}		0	$0.2V_{DDO}$	V
Operating Freq.	f_{OPG1}	Crystal Mode	32	100	kHz
	f_{OPG2}	External RC Mode	32	1000	kHz
	f_{OPG3}	CF Mode	455	3580	kHz

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Electrical Characteristics

Ta=0 to 70℃

Power Consumption

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Consumption (Halt Mode)	I_{Halt1}	32768Hz; BCF=1, #1		2	5	uA
	I_{Halt2}	32768Hz; BCF=1, #2		10	15	uA
	I_{Halt3}	32768Hz; BCF=1, #3		10	15	uA
	I_{Halt4}	32768Hz; BCF=0, #1		2	5	uA
	I_{Halt5}	32768Hz; BCF=0, #2		2	5	uA
	I_{Halt6}	32768Hz; BCF=0, #3		10	15	uA
Power Consumption (Stop Mode)	I_{Stop1}	BCF=1, #1			1	uA
	I_{Stop2}	BCF=1, #2			1	uA
	I_{Stop3}	BCF=1, #3			1	uA

Note: #1: V_{DD1}= 1.5V (Ag), #2: V_{DD2}= 3.0V (Li), #3: V_{DD2}= 3.0V (EXT-V), and without loading.

Input resistance

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
″L″-Level Hold t_R (IOC)	R_{IIH1}	V_I=0.2V_{DD1}, #1	10	40	100	kΩ
	$R_{IIH2\,/\,3}$	V_I=0.2V_{DD2}, #2, #3	10	40	100	kΩ
IOC/IOA Pull-Down t_R	R_{MSD1}	V_I=V_{DD1}, #1	200	500	1000	kΩ
	$R_{MSD2\,/\,3}$	V_I=V_{DD2}, #2, #3	200	500	1000	kΩ
INT Pull-Up t_R	R_{INTU1}	V_I=V_{DD1}, #1	200	500	1000	kΩ
	$R_{INTU2\,/\,3}$	V_I=V_{DD2}, #2, #3	200	500	1000	kΩ
INT Pull-Down t_R	R_{INTD1}	V_I=GND, #1	200	500	1000	kΩ
	$R_{INTD2\,/\,3}$	V_I=GND, #2, #3	200	500	1000	kΩ
RES Pull-Down t_R	R_{RES1}	V_I=GND or V_{DD1}, #1	5	20	50	kΩ
	$R_{RES2\,/\,3}$	V_I=GND or V_{DD2}, #2, #3	5	20	50	kΩ

Note: #1: V_{DD1}= 1.2V (Ag), #2: V_{DD2}= 2.4V (Li), #3: V_{DD2}= 2.4V (EXT-V).

DC output characteristics

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit
Output ″H″ Voltage	V_{OH1a}	I_{OH}= -10μA, #1	SEG1~ SEG32	0.8	0.9	1.0	V
	$V_{OH2a\,/\,3a}$	I_{OH}= -50μA, #2, #3		1.5	1.8	2.1	V
Output ″L″ Voltage	V_{OL1a}	I_{OL}= 20μA, #1		0.2	0.3	0.4	V
	$V_{OL2a\,/\,3a}$	I_{OL}= 100μA, #2, #3		0.3	0.6	0.9	V
Output ″H″ Voltage	V_{OH1c}	I_{OH}= -200μA, #1	SEG33~ SEG42, IOB3~4, IOC1~4	0.8	0.9	1.0	V
	$V_{OH2c\,/\,3c}$	I_{OH}= -1mA, #2, #3		1.5	1.8	2.1	V
Output ″L″ Voltage	V_{OL1c}	I_{OL}= 400μA, #1		0.2	0.3	0.4	V
	$V_{OL2c\,/\,3c}$	I_{OL}= 2mA, #2, #3		0.3	0.6	0.9	V

Note: #1: V_{DD1}= 1.2V (Ag), #2: V_{DD2}= 2.4V (Li), #3: V_{DD2}= 2.4V (EXT-V).

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Segment driver output characteristics

Name	Symbol	Condition	For	Min.	Typ.	Max.	Unit
Static display mode							
Output ″H″ Voltage	V_{OH1d}	I_{OH}= -1μA, #1	SEG-n	1.0			V
	$V_{OH2d / 3d}$	I_{OH}= -1μA, #2, #3		2.2			V
Output ″L″ Voltage	V_{OL1d}	I_{OL}= 1μA, #1				0.2	V
	$V_{OL2d / 3d}$	I_{OL}= 1μA, #2, #3				0.2	V
Output ″H″ Voltage	V_{OH1e}	I_{OH}= -10μA, #1	COM-n	1.0			V
	$V_{OH2e / 3e}$	I_{OH}= -10μA, #2, #3		2.2			V
Output ″L″ Voltage	V_{OL1e}	I_{OL}= 10μA, #1				0.2	V
	$V_{OL2e / 3e}$	I_{OL}= 10μA, #2, #3				0.2	V
1/2 bias display mode							
Output ″H″ Voltage	$V_{OH1f / 2f}$	I_{OH}= -1μA, #1, #2	SEG-n	2.2			V
	V_{OH3f}	I_{OH}= -1μA, #3		2.2			V
Output ″L″ Voltage	$V_{OL1f / 2f}$	I_{OL}= 1μA, #1, #2				0.2	V
	V_{OL3f}	I_{OL}= 1μA, #3				0.2	V
Output ″H″ Voltage	$V_{OH1g / 2g}$	I_{OH}= -10μA, #1, #2	COM-n	2.2			V
	V_{OH3g}	I_{OH}= -10μA, #3		2.2			V
Output ″M″ Voltage	$V_{OM1g / 2g}$	$I_{OI/H}$= ±10μA, #1, #2		1.0		1.4	V
	V_{OM3g}	$I_{OI/H}$= ±10μA, #3		1.0		1.4	V
Output ″L″ Voltage	$V_{OL1g / 2g}$	I_{OL}= 10μA, #1, #2				0.2	V
	V_{OL3g}	I_{OL}= 10μA, #3				0.2	V
1/3 bias display mode							
Output ″H″ Voltage	V_{OH12i}	I_{OH}= -1μA, #1, #2	SEG-n	3.4			V
	V_{OH3i}	I_{OH}= -1μA, #3		3.4			V
Output ″M1″ Voltage	V_{OM12i}	$I_{OI/H}$= ±10μA, #1, #2		1.0		1.4	V
	V_{OM13i}	$I_{OI/H}$= ±10μA, #3		1.0		1.4	V
Output ″M2″ Voltage	V_{OM22i}	$I_{OI/H}$= ±10μA, #1, #2		2.2		2.6	V
	V_{OM23i}	$I_{OI/H}$= ±10μA, #3		2.2		2.6	V
Output ″L″ Voltage	V_{OL12i}	I_{OL}= 1μA, #1, #2				0.2	V
	V_{OL3i}	I_{OL}= 1μA, #3				0.2	V
Output ″H″ Voltage	V_{OH12j}	I_{OH}= -10μA, #1, #2	COM-n	3.4			V
	V_{OH3j}	I_{OH}= -10μA, #3		3.4			V
Output ″M1″ Voltage	V_{OM12j}	$I_{OI/H}$= ±10μA, #1, #2		1.0		1.4	V
	V_{OM13j}	$I_{OI/H}$= ±10μA, #3		1.0		1.4	V
Output ″M2″ Voltage	V_{OM22j}	$I_{OI/H}$= ±10μA, #1, #2		2.2		2.6	V
	V_{OM23j}	$I_{OI/H}$= ±10μA, #3		2.2		2.6	V
Output ″L″ Voltage	V_{OL12j}	I_{OL}= 10μA, #1, #2				0.2	V
	V_{OL3j}	I_{OL}= 10μA, #3				0.2	V

Note: #1: V_{DD1}= 1.2V (Ag), #2: V_{DD2}= 2.4V (Li), #3: V_{DD2}= 2.4V (EXT-V).

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Instruction Table

Instruction	Machine Code	Function	Flag/Remark
NOP	0000 0000 0000 0000	No Operation	
LCT Lz, Ry	0000 001Z ZZZZ YYYY	Lz ← { 7SEG ← Ry}	
LCB Lz, Ry	0000 010Z ZZZZ YYYY	Lz ← { 7SEG ← Ry}	
LCP Lz, Ry	0000 011Z ZZZZ YYYY	Lz ← Ry, AC	
LCD Lz, @HL	0000 100Z ZZZZ 0000	Lz ← T@HL	
SPA X	1101 1100 000X XXXX	X3~0: Set A4~1 I/O X4: Set A4~1 Pull-Low	
SPB X	1101 1101 0000 XXXX	X3~0: Set B4~1 I/O	
SPC X	1101 1110 000X XXXX	X3~0: Set C4-1 I/O X4: Set C4-1 Pull-Low/ Low-Level-Hold	
SPD X	1101 1111 0000 XXXX	X3~0: Set D4~1 I/O	
OPA Rx	0000 1010 0XXX XXXX	Port(A) ← Rx	
OPB Rx	0000 1100 0XXX XXXX	Port(B) ← Rx	
OPC Rx	0000 1101 0XXX XXXX	Port(C) ← Rx	
OPD Rx	0000 1110 0XXX XXXX	Port(D) ← Rx	
IPA Rx	0100 0010 0XXX XXXX	AC, Rx ← Port(A)	
IPB Rx	0100 0100 0XXX XXXX	AC, Rx ← Port(B)	
IPC Rx	0100 0111 0XXX XXXX	AC, Rx ← Port(C)	
IPD Rx	0100 1000 0XXX XXXX	AC, Rx ← Port(D)	
OPAS Rx, D	0000 1011 DXXX XXXX	A1, 2, 3, 4 ← Rx0, Rx1, D, Pulse	
OPDS Rx	0000 1111 DXXX XXXX	D1, 2, 3, 4 ← Rx0, Rx1, D, Pulse	
LDS Rx, D	01011DDD DXXX XXXX	AC, Rx ← D	
STA Rx	0110 1000 0XXX XXXX	Rx ← AC	
STA @HL	0110 1000 1000 0000	@HL ← AC	
LDA Rx	0110 1100 0XXX XXXX	AC ← Rx	
LDA @HL	0100 1100 1000 0000	AC ← @HL	
MRW Ry, Rx	0111 0YYY YXXX XXXX	AC, Ry ← Rx	
MRW @HL, Rx	0110 1110 0XXX XXXX	AC, @HL ← Rx	
MWR Rx, Ry	0111 1YYY YXXX XXXX	AC, Rx ← Ry	
MWR Rx, @HL	0110 1111 0XXX XXXX	AC, Rx ← @HL	
MVL Rx	0001 1100 0XXX XXXX	L ← Rx	
MVH Rx	0001 1101 0XXX XXXX	H ← Rx	
LDH Rx, @HL	0110 0000 0XXX XXXX	AC, Rx ← H(T@HL)	
LDH* Rx, @HL	0110 0001 0XXX XXXX	AC, Rx ← H(T@HL) HL ← HL + 1	
LDL Rx, @HL	0110 0010 0XXX XXXX	AC, Rx ← L(T@HL)	
LDL* Rx, @HL	0110 0011 0XXX XXXX	AC, Rx ← L(T@HL) HL ← @HL + 1	

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Instruction	Machine Code	Function	Flag/Remark
ADC Rx	0010 0000 0XXX XXXX	AC ← Rx + AC + CF	CF
ADC @HL	0010 0000 1000 0000	AC ← @HL + AC + CF	CF
ADC* Rx	0010 0001 0XXX XXXX	AC, Rx ← Rx + AC + CF	CF
ADC* @HL	0010 0001 1000 0000	AC, @HL ← @HL + AC + CF	CF
SBC Rx	0010 0010 0XXX XXXX	AC ← Rx + ACB + CF	CF
SBC @HL	0010 0010 1000 0000	AC ← @HL + ACB + CF	CF
SBC* Rx	0010 0011 0XXX XXXX	AC, Rx ← Rx + ACB + CF	CF
SBC* @HL	0010 0011 1000 0000	AC, @HL ← @HL + ACB + CF	CF
ADD Rx	0010 0100 0XXX XXXX	AC ← Rx + AC	CF
ADD @HL	0010 0100 1000 0000	AC ← @HL + AC	CF
ADD* Rx	0010 0101 0XXX XXXX	AC, Rx ← Rx + AC	CF
ADD* @HL	0010 0101 1000 0000	AC, @HL ← @HL + AC	CF
SUB Rx	0010 0110 0XXX XXXX	AC ← Rx + ACB + 1	CF
SUB @HL	0010 0110 1000 0000	AC ← @HL+ACB+1	CF
SUB* Rx	0010 0111 0XXX XXXX	AC, Rx ← Rx+ACB+1	CF
SUB* @HL	0010 0111 1000 0000	AC,@HL ← @HL+ACB+1	CF
ADN Rx	0010 1000 0XXX XXXX	AC ← Rx + AC	
ADN @HL	0010 1000 1000 0000	AC ← @HL + AC	
ADN* Rx	0010 1001 0XXX XXXX	AC, Rx ← Rx + AC	
ADN* @HL	0010 1001 1000 0000	AC, @HL ← @HL + AC	
AND Rx	0010 1010 0XXX XXXX	AC ← Rx AND AC	
AND @HL	0010 1010 1000 0000	AC ← @HL AND AC	
AND* Rx	0010 1011 0XXX XXXX	AC, Rx ← Rx AND AC	
AND* @HL	0010 1011 1000 0000	AC, @HL ← @HL AND AC	
EOR Rx	0010 1100 0XXX XXXX	AC ← Rx EXOR AC	
EOR @HL	0010 1100 1000 0000	AC ← @HL EXOR AC	
EOR* Rx	0010 1101 0XXX XXXX	AC, Rx ← Rx EXOR AC	
EOR* @HL	0010 1101 1000 0000	AC,@HL ← @HL EXOR AC	
OR Rx	0010 1110 0XXX XXXX	AC ← Rx OR AC	
OR @HL	0010 1110 1000 0000	AC ← @HL OR AC	
OR* Rx	0010 1111 0XXX XXXX	AC, Rx ← Rx OR AC	
OR* @HL	0010 1111 1000 0000	AC,@HL ← @HL OR AC	
ADCI Ry, D	0011 0000 DDDD YYYY	AC ← Ry + D + CF CF	
ADCI* Ry, D	0011 0001 DDDD YYYY	AC, Ry ← Ry + D + CF	CF
SBCI Ry, D	0011 0010 DDDD YYYY	AC ← Ry + DB + CF	CF
SBCI* Ry, D	0011 0011 DDDD YYYY	AC, Ry ← Ry + DB + CF	CF
ADDI Ry, D	0011 0100 DDDD YYYY	AC ← Ry + D	CF
ADDI* Ry, D	0011 0101 DDDD YYYY	AC, Ry ← Ry + D	CF
SUBI Ry, D	0011 0110 DDDD YYYY	AC ← Ry + DB + 1	CF
SUBI* Ry, D	0011 0111 DDDD YYYY	AC, Ry ← Ry + DB + 1	CF

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Instruction	Machine Code	Function	Flag/Remark
ADNI Ry, D	0011 1000 DDDD YYYY	AC ← Ry + D	
ADNI* Ry, D	0011 1001 DDDD YYYY	AC, Ry ← Ry + D	
ANDI Ry, D	0011 1010 DDDD YYYY	AC ← Ry AND D	
ANDI* Ry, D	0011 1011 DDDD YYYY	AC, Ry ← Ry AND D	
EORI Ry, D	0011 1100 DDDD YYYY	AC ← Ry EXOR D	
EORI* Ry, D	0011 1101 DDDD YYYY	AC, Ry ← Ry EXOR D	
ORI Ry, D	0011 1110 DDDD YYYY	AC ← Ry OR D	
ORI* Ry, D	0011 1111 DDDD YYYY	AC, Ry ← Ry OR D	
INC* Rx	0100 0000 0XXX XXXX	AC, Rx ← Rx+1	
INC* @HL	0100 0000 1000 0000	AC, @HL ← @HL+1	
DEC* Rx	0100 0001 0XXX XXXX	AC, Rx ← Rx-1	
DEC* @HL	0100 0001 1000 0000	AC, @HL ← @HL-1	
DAA	0101 0100 0000 0000	AC ← BCD(AC)	
DAA* Rx	0101 0101 0XXX XXXX	AC, Rx ← BCD(AC)	
DAA* @HL	0101 0101 1000 0000	AC, @HL ← BCD(AC)	
DAS	0101 0110 0000 0000	AC ← BCD(AC)	
DAS* Rx	0101 0111 0XXX XXXX	AC, Rx ← BCD(AC)	
DAS* @HL	0101 0111 1000 0000	AC, @HL ← BCD(AC)	
SR0 Rx	0101 0000 0XXX XXXX	ACn, Rxn ← Rx(n+1) AC3, Rx3 ← 0	
SR1 Rx	0101 0001 0XXX XXXX	ACn, Rxn ← Rx(n+1) AC3, Rx3 ← 1	
SL0 Rx	0101 0010 0XXX XXXX	ACn, Rxn ← Rx(n-1) AC0, Rx0 ← 0	
SL1 Rx	0101 0011 0XXX XXXX	Can, Rxn ← Rx(n-1) AC0, Rx0 ← 1	
MAF Rx	0100 1010 0XXX XXXX	AC, Rx ← STS 1	B3: CF B2: AC=0 B1: (No use) B0: (No use)
MSB Rx	0100 1011 0XXX XXXX	AC, Rx ← STS 2	B3: (No use) B2: SCF 2 (HRx) B1: SCF 1 (CPT) B0: BCF
MSC Rx	0100 1100 0XXX XXXX	AC, Rx ← STS 3	B3: SCF 7 (PDV) B2: PH15 B1: SCF 5 (TMR1) B0: SCF 4 (INT)
MCX Rx	0100 1101 0XXX XXXX	AC, Rx ← STS 3X	B3: SCF 9 (RFC) B2: SCF 0 (APT) B1: SCF 6 (TMR2) B0: (No use)
MSD Rx	0100 1110 0XXX XXXX	AC, Rx ← STS 4	B3: (No use) B2: RFOVF B1: WDF

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Instruction	Machine Code	Function	Flag/Remark
			B0: CSF
MDX Rx	0100 1111 0XXX XXXX	AC, Rx ← STS 4X	B3: ADF 4 B2: ADF 3 B1: ADF 2 B0: ADF 1
MRA Rx	0110 1101 0XXX XXXX	CF ← Rx3	CF
MRF1 Rx	0110 0100 0XXX XXXX	AC, Rx ← RFC 3-0	
MRF2 Rx	0110 0101 0XXX XXXX	AC, Rx ← RFC 7-4	
MRF3 Rx	0110 0110 0XXX XXXX	AC, Rx ← RFC 11-8	
MRF4 Rx	0110 0111 0XXX XXXX	AC, Rx ← RFC 15-12	
JB0 X	1000 0XXX XXXX XXXX	PC ← X	If AC0 = 1
JB1 X	1000 1XXX XXXX XXXX	PC ← X	If AC1 = 1
JB2 X	1001 0XXX XXXX XXXX	PC ← X	If AC2 = 1
JB3 X	1001 1XXX XXXX XXXX	PC ← X	If AC3 = 1
JZ X	1011 0XXX XXXX XXXX	PC ← X	If AC = 0
JNZ X	1010 0XXX XXXX XXXX	PC ← X	If AC ≠ 0
JC X	1011 1XXX XXXX XXXX	PC ← X	If CF = 1
JNC X	1010 1XXX XXXX XXXX	PC ← X	If CF = 0
JMP X	1101 0XXX XXXX XXXX	PC ← X	
CALL X	1100 0XXX XXXX XXXX	STACK ← PC+1 PC ← X	
RTS	1101 1000 0000 0000	PC ← STACK	Return from CALL
SCC X	1101 1001 0X0X 0XXX	X6: 0 PH0, 1 BCLK	FREQ CLK Source
		X5: 0 PH0, 1 BCLK	PWM CLK Source
		X4: 0 Port C, 1 Port A	Chattering Prevention Clock
		X2, 1, 0: 001 PH10, 010 PH8, 100 PH6	
SAD X	1101 1011 00XX XXXX	X5: Enable Cmp. output X4: Latch Data to Cmp. X3=0: CP4 (+) = AN4 X2=1: CP1~4 (-) = AN4 X2=0: CP1~4 (-) = DAC X0: Enable DAC	
MDA Rx	1110 0011 0XXX XXXX	DAC ← Rx	
MPW1 Rx	0001 1110 0XXX XXXX	PWM1 ← Rx , AC	
MPW2 Rx	0001 1111 0XXX XXXX	PWM2 ← Rx , AC	
FRQ D, Rx	0001 00DD 0XXX XXXX	FREQ ← Rx, AC	DD=00: 1/2 Duty DD=01: 1/3 Duty DD=10: 1/4 Duty
FRQ D, @HL	0001 01DD 0000 0000	FREQ ← T@HL	
FRQX D, X	0001 10DD XXXX XXXX	FREQ ← X	
TMS Rx	1110 0000 0XXX XXXX	Timer1 ← Rx, AC	
TMS @HL	1110 0001 0000 0000	Timer1 ← T@HL	
TMS X	1110 0010 XXXX XXXX	X7, 6: 00 PH9, 01 PH3, 10 PH15, 11 FREQ	
		X5~0: Set Timer1 Value	

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Instruction	Machine Code	Function	Flag/Remark
TM2 Rx	1110 0100 0XXX XXXX	Timer2←Rx, AC	
TM2 @HL	1110 0101 0000 0000	Timer2←T@HL	
TM2X X	1110 011X XXXX XXXX	X8, 7, 6: 000 PH9 / 001 PH3 / 010 PH15 / 011 FREQ / 100 PH5 / 101 PH7 / 110 PH11 / 111 PH13 X5~0: Set Timer2 Value	
SRF X	1110 1100 00XX XXXX	X5: Enable Cx Control X4: Enable Timer2 Control X3: Enable Counter X2: Enable RH Output X1: Enable RT Output X0: Enable RR Output	
SHE X	1110 1000 0XXX XXX0	X6: Enable HEF 6 (RFC) X4: Enable HEF 4 (TMR 2) X3: Enable HEF 3 (Pre-Divider) X2: Enable HEF 2 (INT) X1: Enable HEF 1 (TMR 1)	
SIE* X	1110 1001 0XXX XXXX	X6: Enable IEF 6 (RFC) X4: Enable IEF 4 (TMR2) X3: Enable IEF 3 (Pre-Divider) X2: Enable IEF 2 (INT) X1: Enable IEF 1 (TMR1) X0: Enable IEF 0 (A / C Port)	
SCA X	1101 1010 00XX 0000	X5: A1-4 Enable (SEF 5) X4: C1-4 Enable (SEF 4)	
SRE X	1110 1101 0XXX 0000	X6~4: Enable SRF6~4	SRF6 (A Port) SRF5 (INT Pin) SRF4 (M Port)
PLC X	1110 101X 0XXX XXXX	X8: Reset PH15~11 X6, 4~0: Reset HRF6, 4~0	
SF X	1111 0000 X00X XXXX	X7: Reload Set X4: WDT Enable X3: HALT after EL LIGHT X2: EL LIGHT On X1: BCF Set X0: CF Set	RL1 WDF BCF CF
SF2 X	1111 1000 0000 0XXX	X0: Reload Set X1: Dis-ENX Set X2: Close all segments	RL2 DED RSOFF
RF X	1111 0100 X00X 0XXX	X7: Reload Reset X4: WDT Reset X2: EL LIGHT Off X1: BCF Reset X0: CF Reset	RL1 WDF BCF CF
RF2 X	1111 1001 0000 0XXX	X0: Reload Reset X1: Dis-ENX Reset X2: Release all Segments	RL2 DED RSOFF

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Instruction	Machine Code	Function					Flag/Remark
ALM X	1111 101X XXXX XXXX	X8, 7, 6	000 001 010	DC0 PH5 PH4	011 100 111	PH3 DC1 FREQ	
		X5~0	PH15~10				
ELC X	1111 110X XXXX XXXX	X8, 7, 6	000 100 101	PH0 BCLK BCLK/2	110 111	BCLK/4 BCLK/8	ELP – Pumping Clock Source
		X5, 4	00 01	1/4 Duty 1/3 Duty	10 11	1/2 Duty 1/1 Duty	ELP – Duty Cycle
		X3, 2	00 01	PH8 PH7	10 11	PH6 PH5	ELC – Discharge Pulse Frequency
		X1, 0	00 01	1/4 Duty 1/3 Duty	10 11	1/2 Duty 1/1 Duty	ELC – Duty Cycle
FAST	1110 1110 0000 0000	SCLK: High Speed Clock					
SLOW	1110 1111 0000 0000	SCLK: Low Speed Clock					
HALT	1111 1110 0000 0000	HALT operation					
STOP	1111 1111 0000 0000	STOP operation					

Symbol description

AC:	Accumulator	ACn:	Accumulator bit-n
PC:	Program counter	CF:	Carry flag
X:	Address	D:	Immediate data
Rx:	Memory of address X	Rxn:	Memory bit-n of address X
Ry:	Memory of working register Y	CSF:	Clock source flag
WDF:	Watchdog timer enable flag	BCF:	Back-up flag
BCLK:	System clock address	SEFn:	Switch enable flag
IEFn:	Interrupt enable flag	HRFn:	HALT release flag
SRFn:	Stop release enable flag	HEFn:	HALT release enable flag
SCFn:	Start condition flag	TMR:	Timer overflow release flag
RFOVF:	RFC overflow flag	ADF:	ADC flag
DAC:	Digital-to-analog converter output signal	Lz:	LCD latch
FREQ:	Frequency generator setting value	H:	High address of index
HL:	Index register	L:	Low address of index
@HL:	Memory of index RAM	HT@HL:	High nibble of index ROM
T@HL:	Memory of index ROM	LT@HL:	Low nibble of index ROM
LBR:	Low-battery voltage reference		

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Mask option table

ITEM	Description	OPTION-1	OPTION-2	OPTION-3	OPTION-4 OPTION-5
1	POWER SOURCE	EXT-V	LI	AG	
2	CLOCK SOURCE	FAST ONLY	SLOW ONLY	DUAL	
3	FAST CLOCK TYPE	X'TAL	RC	NO USE	
4	INT PIN INTERNAL RESISTOR	PULL HIGH	PULL LOW	OPEN TYPE	
5	INT PIN TRIGGER MODE	RISING EDGE	FALLING EDGE		
6	LCD / LED	LCD	LED HIGH ACTIVE	LED LOW ACTIVE	
7	LCD DISPLAY IN RESET CYCLE	ON	OFF		
8	F SEGMENT FOR DISPLAY "7"	ON	OFF		
9	LCD/LED FRAME FREQUENCY	—	TYPICL(*)	FAST(**)	
10	LCD BIAS	1/3 BIAS	1/2 BIAS		
11	LCD/LED DUTY CYCLE	O/P	STATIC	DUPLEX	1/3 DUTY 1/4 DUTY
12	WATCH DOG TIMER OVERFLOW TIME INTERVAL	8/PH10	64/PH10	512/PH10	
13	C PORT LOW LEVEL HOLD	USE	NO USE		
14	PWM1,PWM2 COUNT	N/63	N/255	NO USE	
15	SEG33/IOD1	SEG33	IOD1		
16	SEG34/IOD2	SEG34	IOD2		
17	SEG35/IOD3/PWM1	SEG35	IOD3	PWM1	
18	SEG36/IOD4/PWM2	SEG36	IOD4	PWM2	
19	SEG37/IOA1/CX	SEG37	IOA1	CX	
20	SEG38/IOA2/RR	SEG38	IOA2	RR	
21	SEG39/IOA3/RT	SEG39	IOA3	RT	
22	SEG40/IOA4/RH	SEG40	IOA4	RH	
23	SEG41/IOB1/ELC	SEG41	IOB1	ELC	
24	SEG42/IOB2/ELP	SEG42	IOB2	ELP	
25	IOB3/BZB	IOB3	BZB		
26	IOB4/BZ	IOB4	BZ		
27	IOC1/AN1	IOC1	AN1		
28	IOC2/AN2	IOC2	AN2		
29	IOC3/AN3	IOC3	AN3		
30	IOC4/AN4	IOC4	AN4		

Note : 1.(*) If the LCD frequency select “Typical(32.0Hz)”, the LCD panel will happen flash problem possible.

2. (**) If the LCD frequency option from “Typical” to “Fast”, the LCD panel consumer current will increase double. (Refer JA54270 User manual)

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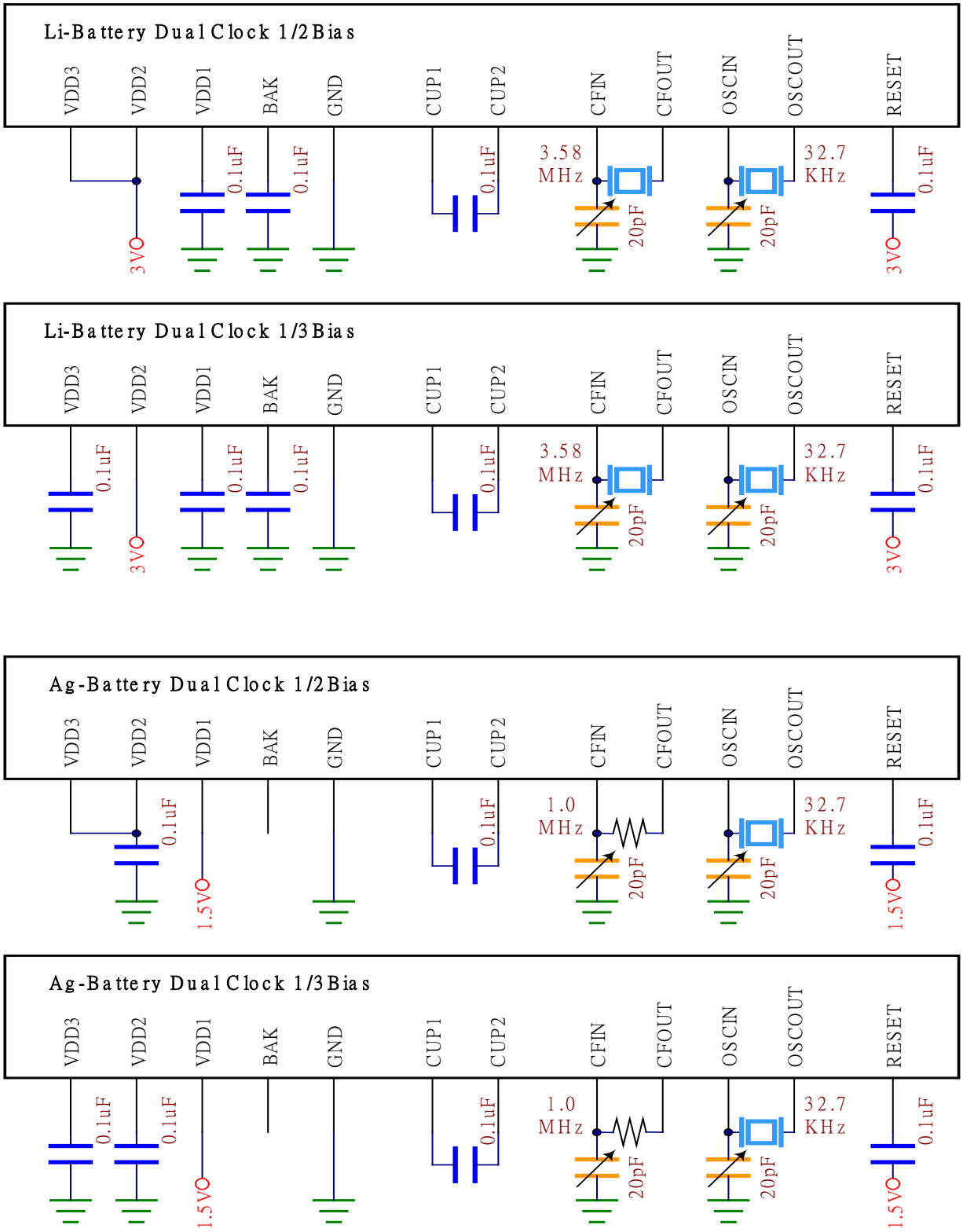
Application Circuit



Note: This application circuit is simply for reference and not guaranteed to work.

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JA54270 Preliminary SPEC

Revision History

Version	Date	Comment
0.0	2004/03/01	Original version.
0.2	2004/10/01	Supply voltage VDD minmum 1.1V -> 1.2V.
0.3	2004/11/11	Add a warning : Warning :The JA54270 chip's LBR function was cancelled since 2004/11/11.
0.4	2005/05/25	Add important issue. (Refer Page.17~18)
0.5	2005/10/01	Remove important issue. (Refer the JA54270 UM).
0.6	2005/12/05	Modify Mask Option table and note.

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