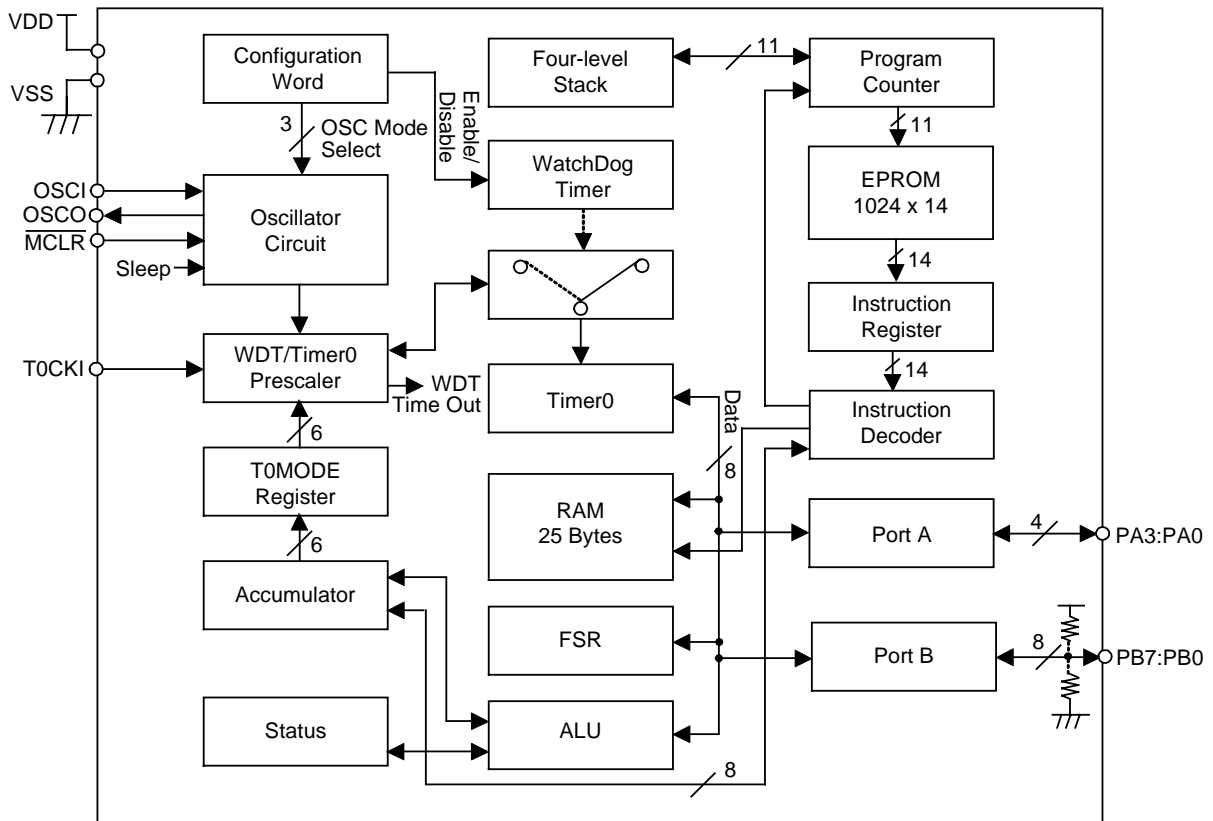
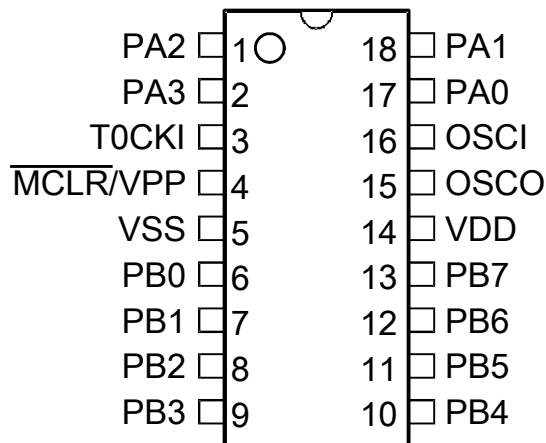

EPROM-Based 8-Bit CMOS Microcontroller**General Description**

JA5856F is an 8-bit microcontroller that employs enhanced EPROM technology with low cost, high speed and high noise immunity. Watchdog Timer, RAM, EPROM, I/O port, power down mode, and real time programmable clock/counter are integrated into this chip. JA5856F contain 33 instructions. All are single cycle except for program branches that take two cycles. On chip memory is available with 1K x 14 bits ROM and 25 bytes RAM.

Features

- Total 33 single word instructions.
- The fast execution time may be 200ns for all single cycle instructions under 20MHz operation.
- Operating voltage range:
Normal: 2.4V ~ 5.5V; HSXTAL: 3.5V ~ 5.5V
- Operating temperature: -20 °C ~ 85 °C
- ROM size: 1K x 14 bits
- RAM size: 25 bytes
- Stack: 4 level
- 8 bits real time clock/counter with 8 bits programmable Prescaler.
- Internal Power-on Reset and built-in LVDT circuit (Low Voltage Detector) selected by option.
- On chip Watch Dog Timer (WDT) based on internal RC oscillator.
- Direct and indirect addressing modes for data accessing.
- Sleeping Mode for power saving.
- 8 types of oscillators selected by option:
 - HSXTAL: High speed crystal
 - XTAL: Standard crystal
 - LPXTAL1: Low power crystal in noise immunity
 - LPXTAL2: Low power crystal in power saving
 - RC1: External high-speed RC
 - RC2: External low-speed RC
 - RC3: Internal 4MHz fixed RC
 - RC4: Internal 455kHz fixed RC
- PORTA and PORTB have 12 I/O pins with independent direction control
- PORTB with pin change wake-up function selected by option
- PORTB with pull high/low resistors selected by option

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Block Diagram

Pin Assignment (PDIP-18PIN / SOP-18PIN)

JA5856F

Pin Description

Pin Name	Pin Number	Pin Type	Buffer Type	Description
PA0	17	I/O	CMOS	Bi-directional I/O port.
PA1	18			
PA2	1			
PA3	2			
PB0	6	I/O	CMOS	Bi-directional I/O port with pin Wake-up functions pull high/low resistors selected by option.
PB1	7			
PB2	8			
PB3	9			
PB4	10			
PB5	11			
PB6	12			
PB7	13			
T0CKI/SCL	3	I	ST	Input to Timer0. If unused, it must be tied to V _{DD} or V _{SS} .
$\overline{\text{MCLR}}/\text{V}_{\text{PP}}$	4	I	ST	Reset/programming voltage input. The pin is an active low Reset with build-in LVDT circuit (low voltage detector) selected by option. Voltage on the pin must not exceed V _{DD} to avoid unintended entering Programming Mode.
OSCI	16	I	ST	Oscillator input.
OSCO	15	O	-	Oscillator output. At RC mode, this pin will output 1/4 frequency of OSCI to denote the cycle rate for instruction.
V _{DD}	14	P	-	Positive power supply.
V _{SS}	5	P	-	Ground

Note:

Legend: I = input, I/O = input/output, P = power, - = not used, CMOS = CMOS, ST = Schmitt Trigger

Register Organization

Register Map

Address	Name	Description
00H	INAR	Indirect Address Register
01H	Timer0	8-bit real-time clock/timer
02H	PC	Program Counter
03H	STATUS	STATUS Register
04H	FSR	File Select Register
05H	PORTA	I/O Register
06H	PORTB	I/O Register
07H~1FH	General Purpose Registers	General Purpose Registers

INAR (Indirect Address Register): 00H

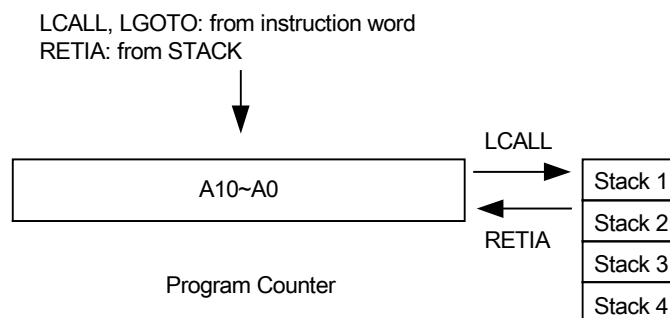
This Register is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction accessing this register can access data pointed by FSR (04H).

Timer0 (8-bit real-time clock/timer): 01H

This register increases by an external signal edge applied to T0CKI pin, or by internal instruction cycle. It can be read or written as any other register.

PC (Program Counter): 02H

This register increases itself along with every instruction cycle, except the following condition specified as below:



STATUS (STATUS Register): 03H

Bit	Symbol	Name	Description
0	C	Carry/Borrow bit.	for <i>ADDAR</i> instruction 1 - A carry occurred 0 - A carry did not occur for <i>SUBAR</i> instruction 1 - A borrow did not occur 0 - A borrow occurred
1	DC	Digit carry/borrow bit	for <i>ADDAR</i> instruction 1 - A carry from the 4th low order bit of the result occurred 0 - A carry from the 4th low order bit of the result did not occur for <i>SUBAR</i> instruction 1 - A borrow from the 4th low order bit of the result did not occur 0 - A borrow from the 4th low order bit of the result occurred
2	Z	Zero bit.	1 - The result of a logic operation is zero 0 - The result of a logic operation is not zero
3	\overline{PD}	Power-down bit.	1 - After power-up or by the CLRWDT instruction 0 - By the SLEEP instruction
4	\overline{TO}	Time-out bit.	1 - After power-up or by the CLRWDT or SLEEP instruction 0 - A WDT time-overflow occurred
5~7	-	Reserved	

FSR (File select register pointer): 04H

In JA5856F, Bit 0~4 are used to select up to 32 registers (address: 00h~1Fh) and Bit 5~7 were fixed 1. Using the indirect addressing mode show as below:

B 7	B 6	B 5	B 4	B 3	B 2	B 1	B 0
1	1	1	Indirect Address mode location select				

(FSR Content)		Real Address
1110 0000	INAR	00
1110 0001	TIMER0	01
1110 0010	PC	02
1110 0011	STATUS	03
1110 0100	FSR	04
1110 0101	PORT A	05
1110 0110	PORT B	06
1110 0111	General Purpose Register	07
1111 1111		1F

Data Memory Configuration for JA5856F

PORTA: 05H

PA3 PA0: Bi-directional I/O Register.

PORTB: 06H

PB7 PB0: Bi-directional I/O Register. Each pin of PORTB has build-in pull high/low resistor and pin change wake up function that can be select by option independently. Pull high/low resistors and pin change wake up function will enable when user set the I/O pin to input mode and will be disable when it change to output mode. When user use these functions, you must attention something as below :

1. **User should select WDT or pin change wake up function individually. In case of pin change wake up enable, WDT must disable. When system wake up by the PORTB pin level change, the instruction located after the SLEEP will be executed.**
2. **When user want to use the pin change wake up function, it must assign 0FH to Prescalar before execute the "SLEEP" instruction. Therefore, user must take care the switching of Prescalar.**
3. **When system in the Sleeping Mode, the wake up function will happen in case of pin level changed.**
4. **If user had wake up the chip by I/O pin, please mind the chartering (Bounce) to prevent system mal-function. Please note that the pin change wake-up will delivered by the rising or falling signal changed.**

Example:
Configuration word:

WDT: **Disable**
 PORTB pull high resistors: **Disable**
 PORTB pull low resistors: **PB0、PB1**
 PORTB pin change wake up: **PB0**

Source code:

```

.....
CLRA
T0MODE
IOST      PORTA      ; Assign Prescaler to Timer0
IOST      PORTB      ; All pins of PORTA were set to output.
              ; All pins of PORTB were set to output. Pull low resistor ( PB0、 PB1 )
              ; and pin change wake up function ( PB0 ) will be disable.
.....

MOVIA     03H        ; PB0 and PB1 were set to input mode. The pull low resistors and
IOST      PORTB      ; Pin change wake up function were enable

.....
MOVIA     0FH        ; Assign 0FH to Prescalar
T0MODE
SLEEP
CLRA
T0MODE
LCALL     DELAY      ; Assign Prescalar return Timer0
              ; Add a delay for bounce
.....
MOVIA     0FH        ; Assign 0FH to Prescalar
T0MODE
SLEEP
  
```

Description:

When the chip was go into sleep mode, the chip is still in the sleep mode even the PB1 had pin level change. If **PB0** had pin level change, the chip will wake up and execute the next instruction that " CLRA ".

IOST (Control Port I/O Mode Register)

The IOST register is write-only and will be set as '1' upon RESET.

IOST Bit-X = 0; I/O Pin-X Set as output mode.

IOST Bit-X = 1; I/O Pin-X Set as input mode.

T0MODE Register:

T0MODE is a write-only register and the content was be listed as below:

Bit	Symbol	Description		
		Bit Value	Timer Rate	WDT Ratev
2~0	PS2 PS0	0 0 0	1:2	1:1
		0 0 1	1:4	1:2
		0 1 0	1:8	1:4
		0 1 1	1:16	1:8
		1 0 0	1:32	1:16
		1 0 1	1:64	1:32
		1 1 0	1:128	1:64
		1 1 1	1:256	1:128
3	PSC	Prescaler assign bit: = 0 (Timer0) = 1 (WDT)		
4	TE	Timer0 source signal edge select bit: = 0 (Increment when low-to-high transition on T0CKI pin) = 1 (Increment when high-to-low transition on T0CKI pin)		
5	TS	Timer0 source signal select bit: = 0 (Internal instruction clock cycle) = 1 (Transition on T0CKI pin)		
6~7	-	Reserved		

Timer0

Timer0 is an 8-bit timer/counter. The clock source of Timer0 could be come from the internal clock or by an external clock source presented by the T0CKI pin.

To select the internal clock source, bit 5 of the T0MODE register should be clear. In this mode, Timer0 increases by 1 in every instruction cycle (without Prescalar).

To select the external clock source, bit 5 of the T0MODE register should be set. In this mode, Timer0 increases by 1 on every falling or rising edge of T0CKI pin which is be controlled by bit 4 of T0MODE register.

Prescalar

The 8-bit Prescalar may be assigned to either the Timer0 or the WDT through the PSC bit (bit 3 of the T0MODE register). Set this bit to "1" is assigned the Prescalar to the WDT. Set this bit to "0" is assigned the Prescalar to the Timer0. The PS2:PS0 bits determine the Pre-scale ratio. The Prescalar can't be assigned to both the Timer0 and WDT simultaneously.

RESET

This device may be reset by one of the following ways:

- (1) Power-on Reset: At power-up, this device is kept in a RESET condition for a period of 18ms (@5V, Typ.) after the voltage on MCLR pin has reached a logic high level.
- (2) $\overline{\text{MCLR}}$ reset (normal operation).
- (3) WDT reset (normal operation).
- (4) MLR wake-up (from sleep mode).
- (5) WDT wake-up (from sleep mode): Executing the SLEEP instruction can force this device to enter sleep mode (power saving mode). While in sleep mode, the WDT is cleared but keeps running. This device can be awakened by WDT time-out or reset input on $\overline{\text{MCLR}}$ pin.

The contents of registers after reset are listed as below:

Address	Register	Power-On Reset	$\overline{\text{MCLR}}$ or WDT Reset
00h	INAR	xxxx xxxx	uuuu uuuu
01h	Timer0	xxxx xxxx	uuuu uuuu
02h	PC	1111 1111	1111 1111
03h	STATUS	0001 1xxx	000# #uuu
04h	FSR	1xxx xxxx	1uuu uuuu
05h	PORTA	---- xxxx	---- uuuu
06h	PORTB	xxxx xxxx	uuuu uuuu
07h-1Fh	General Purpose Registers	xxxx xxxx	uuuu uuuu
N/A	Acc	xxxx xxxx	uuuu uuuu
N/A	IOST	1111 1111	1111 1111
N/A	T0MODE	-- 11 1111	-- 11 1111

Note:

"x" = unknown

"u" = unchanged

"-" = unimplemented, read as "0"

"#" = refer to the following tables

The STATUS (03H) Register situation for different conditions:

Condition	STATUS: bit 4 ($\overline{\text{TO}}$)	STATUS: bit 3 ($\overline{\text{PD}}$)
$\overline{\text{MCLR}}$ Reset (not during SLEEP)	u	u
$\overline{\text{MCLR}}$ Reset during SLEEP	1	0
WDT Reset (not during SLEEP)	0	1
WDT Reset during SLEEP	0	0

Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator. This RC oscillator is separated from the RC oscillator of the OSC1 pin. That means the WDT keeps running even when the oscillator driver is turned off, such as in sleep mode. During normal operation or in sleep mode, a WDT time-out causes the device reset and the \overline{TO} bit (bit 4 of STATUS register) was cleared.

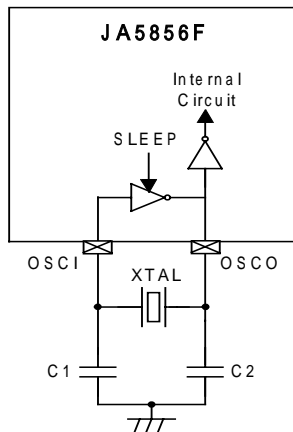
Without Prescaler, the WDT time-out period is 18ms (@5V,Typ.). This period can increase by using the Prescaler. The division ratio of Prescaler is up to 1:128. Thus, the longest time-out period is approximately 2.3s.

Oscillator Configuration

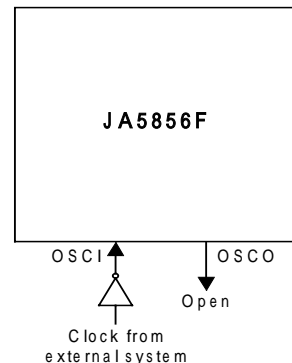
This device supports 8 oscillator modes. Users can select the appropriate mode by compile tool. These oscillator modes offered as:

- HSXTAL: High-speed crystal oscillator with Range from 4MHz to 20MHz
- XTAL: Standard crystal oscillator with Range up to 4MHz
- LPXTAL1: Low power crystal oscillator in noise immunity
- LPXTAL2: Low power crystal oscillator in power saving
- RC1: External Hi-speed RC oscillator with Range from 1MHz to 10MHz
- RC2: External Low-speed RC oscillator with Range from 32kHz to 1MHz
- RC3: Internal 4MHz fixed RC oscillator (3.8MHz up/down 20%)
- RC4: Internal 455kHz fixed RC oscillator (440K up/down 20%)

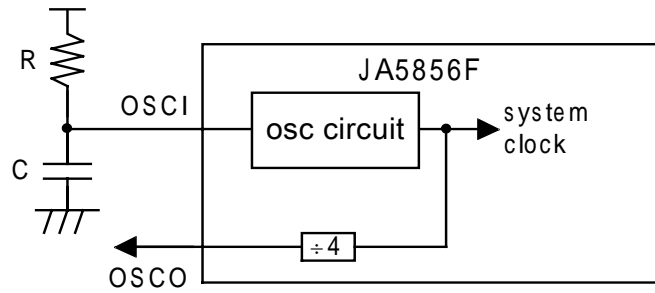
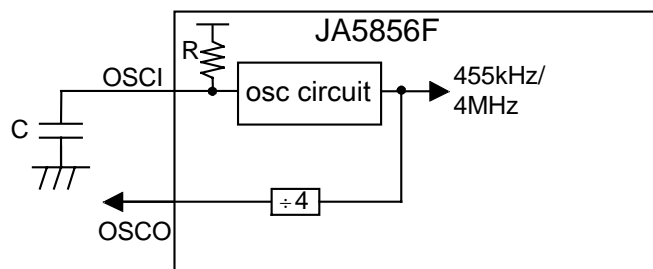
XTAL, HFXTAL or LFXTAL modes



(a) Crystal operation (or ceramic resonator)



(b) External clock input operation

External RC Oscillator Mode

Internal RC Oscillator Mode


Instruction Table

Mnemonic Operands	Description	Cycles	Instruction Code	STATUS Affected
BCR R, bit	Clear bit in R	1	11 11bb brrr rrrr	None
BSR R, bit	Set bit in R	1	11 10bb brrr rrrr	None
BTRSC R, bit	Test bit in R and skip if clear	1 or 2(skip)	11 01bb brrr rrrr	None
BTRSS R, bit	Test bit in R and skip if set	1 or 2(skip)	11 00bb brrr rrrr	None
CLRWDT	Clear Watchdog Timer	1	01 0000 0000 0001	\overline{TO} , \overline{PD}
T0MODE	Load T0MODE Register	1	01 0000 0000 0010	None
SLEEP	Go into standby mode	1	01 0000 0000 0011	\overline{TO} , \overline{PD}
IOST R	Load IOST Register	1	01 0000 0000 0rrr	None
ANDIA I	AND immediate with Acc	1	00 1001 iiii iiii	Z
XORIA I	Exclusive OR immediate with Acc	1	00 1000 iiii iiii	Z
MOVIA I	Move immediate to Acc	1	00 0001 iiii iiii	None
IORIA I	Inclusive OR immediate with Acc	1	00 0011 iiii iiii	Z
RETIA I	Return, place immediate in A	2	00 1100 iiii iiii	None
LCALL I	Call subroutine	2	10 0iii iiii iiii	None
LGOTO I	Unconditional branch	2	10 1iii iiii iiii	None
NOP	No operation	1	01 0000 0000 0000	None
MOVAR R	Move Acc to R	1	01 0000 1rrr rrrr	None
COMR R, d	Complement R	1	01 0010 drrr rrrr	Z
MOVR R, d	Move R	1	01 0011 drrr rrrr	Z
RRR R, d	Rotate right R	1	01 1110 drrr rrrr	C
RLR R, d	Rotate left R	1	01 1100 drrr rrrr	C
SWAPR R, d	Swap halves R	1	01 1101 drrr rrrr	None
CLRA	Clear Acc	1	01 0001 0000 0000	Z
CLRR R	Clear R	1	01 0001 1rrr rrrr	Z
INCR R, d	Increment R	1	01 1000 drrr rrrr	Z
INCRSZ R, d	Increment R, Skip if 0	1 or 2(skip)	01 1001 drrr rrrr	None
DECR R, d	Decrement R	1	01 0110 drrr rrrr	Z
DECRSZ R, d	Decrement R, Skip if 0	1 or 2(skip)	01 0111 drrr rrrr	None
SUBAR R, d	Subtract Acc from R	1	01 1010 drrr rrrr	C, DC, Z
XORAR R, d	Exclusive OR Acc with R	1	01 1011 drrr rrrr	Z
ANDAR R, d	AND Acc with R	1	01 0100 drrr rrrr	Z
ADDAR R, d	Add Acc and R	1	01 0101 drrr rrrr	C, DC, Z
IORAR R, d	Inclusive OR Acc with R	1	01 1111 drrr rrrr	Z

Note:

b : Bit position WDT : Watchdog Timer R : Register address
 i : Immediate data Acc : Accumulator T0MODE : T0MODE register
 \overline{PD} : Power down flag \overline{TO} : Time overflow bit IOST : I/O port status register
 Z : Zero flag C : Carry flag DC : Digital carry flag
 I : ($i_7 i_6 i_5 i_4 i_3 i_2 i_1 i_0$) R : ($r_6 r_5 r_4 r_3 r_2 r_1 r_0$)

D \in [0,1] Destination:
 If d is "0", the result is stored in the Acc register.
 If d is "1", the result is stored back in register R.

Absolute Maximum Ratings

Parameter	Max.	Unit
Storage temperature	-65 to +150	°C
Operation temperature	-20 to +85	°C
Voltage on any pin with respect to V _{ss}	-0.3 to (V _{DD} + 0.3)	V
Voltage on V _{DD} with respect to V _{ss}	-0.3 to +7.5	V

Note:


Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

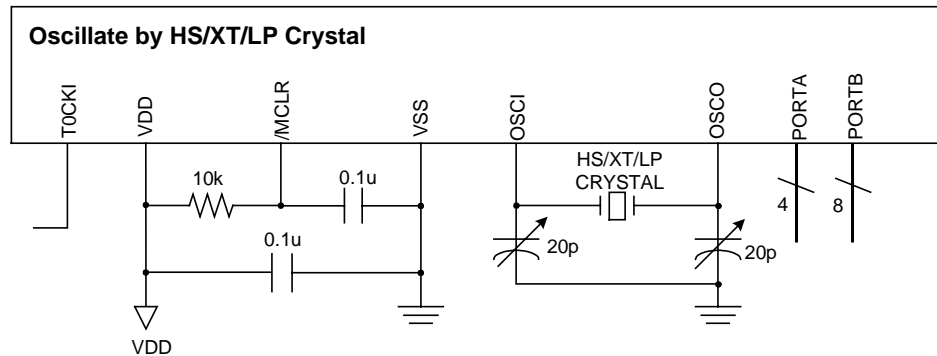
Electrical Characteristics


Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	
Operating Voltage	V _{DD}		2.4		5.5	V	
Input High Voltage	V _{IH}	I/O port, V _{DD} =5V	2.5		V _{DD}	V	
		MCLR, V _{DD} =5V	3.0		V _{DD}	V	
Input Low Voltage	V _{IL}	I/O port, V _{DD} =5V	V _{SS}		2.0	V	
		MCLR, V _{DD} =5V	V _{SS}		1.5	V	
Output Voltage	V _{OH}	V _{DD} =5V, I _{OH} =10mA	3.5			V	
	V _{OL}	V _{DD} =5V, I _{OL} =10mA			1.5	V	
HSXTAL: 20MHz; WDT disable; LVDT disable							
Operating Current	I _{DD}	V _{DD} =5.0V		4.0	5.5	mA	
		V _{DD} =3.0V		1.5	2.0	mA	
HSXTAL: 12MHz; WDT disable; LVDT disable							
Operating Current	I _{DD}	V _{DD} =5.0V		3.0	4.5	mA	
		V _{DD} =3.0V		0.9	1.5	mA	
XTAL: 4MHz; WDT disable; LVDT disable							
Operating Current	I _{DD}	V _{DD} =5.0V		2.0	3.5	mA	
		V _{DD} =3.0V		0.6	1.0	mA	
LPXTAL1: 32KHz; WDT disable; LVDT disable							
Operating Current	I _{DD}	V _{DD} =5.0V		150	200	uA	
		V _{DD} =3.0V		40	55	uA	
LPXTAL2: 32KHz; WDT disable; LVDT disable							
Operating Current	I _{DD}	V _{DD} =5.0V		35	50	uA	
		V _{DD} =3.0V		9.5	15	uA	
RC1: R= 62KOhm; C_{osc1}=100pF; WDT disable; LVDT disable							
Operating Current	I _{DD}	V _{DD} =5.0V	F=1.2MHz		1500	2500	uA
		V _{DD} =3.0V	F=1.3MHz		450	650	uA
RC1: R= 4.7KOhm; C_{osc1}=100pF; WDT disable; LVDT disable							
Operating Current	I _{DD}	V _{DD} =5.0V	F=11MHz		3000	5000	uA
		V _{DD} =3.0V	F=9.7MHz		1000	2000	uA
RC2: R= 1MOhm; C_{osc1}=100pF; WDT disable; LVDT disable							
Operating Current	I _{DD}	V _{DD} =5.0V	F=110KHz		200	250	uA
		V _{DD} =3.0V	F=110KHz		35	50	uA

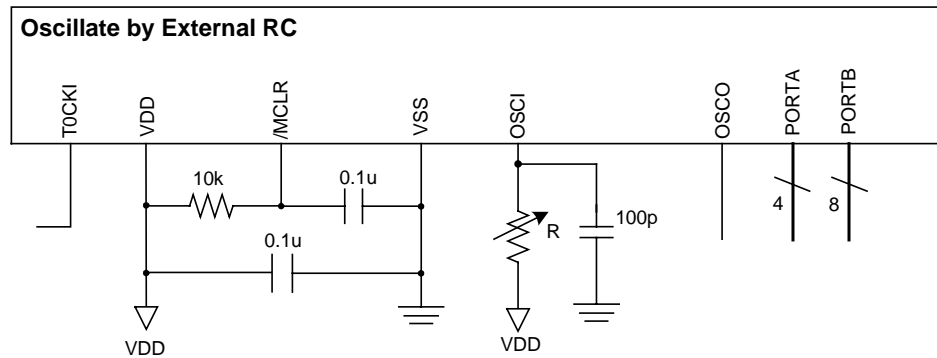
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	
RC2: R= 62KOhm; Cosci=100pF; WDT disable; LVDT disable							
Operating Current	IDD	VDD=5.0V	F=1.6MHz		400	600	uA
		VDD=3.0V	F=1.6MHz		150	200	uA
RC3: Internal 4MHz							
Operating Current	IDD	VDD=5.0V	F=3.8MHz		2.0	2.5	mA
		VDD=3.0V	F=3.9MHz		0.6	0.9	mA
RC4: Internal 455KHz							
Operating Current	IDD	VDD=5.0V	F=440KHz		200	350	uA
		VDD=3.0V	F=460KHz		60	90	uA
Power Down Mode; WDT disable; LVDT disable							
Operating Current	IDD	VDD=5.0V			0.8	1.1	uA
		VDD=3.0V			0.5	0.8	uA
Power Down Mode; WDT disable; LVDT enable							
Operating Current	IDD	VDD=5.0V			3.0	4.5	uA
		VDD=3.0V			2.0	3.5	uA
Power Down Mode; WDT enable; LVDT disable							
Operating Current	IDD	VDD=5.0V			15	25	uA
		VDD=3.0V			4.5	7.0	uA
Internal WDT RC; Prescaler = 1:1							
Watch Dog Timer	T _{WDT}	VDD=5.0V		12	18	30	ms
		VDD=3.0V		15	22	33	ms
Sink current: 4MHz; WDT enable; without LVDT							
I/O Sink Current	I _{OL}	VDD=5.0V, @V _{OL} =0.1V _{DD}		15	25		mA
Source current: 4MHz; WDT enable; without LVDT							
I/O Source Current	I _{OH}	VDD=5.0V, @V _{OL} =0.9V _{DD}		6.0	9.5		mA


Application Circuit

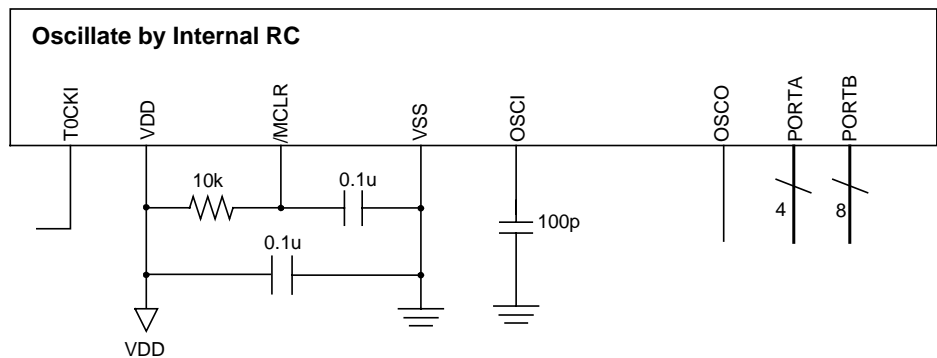
1. External signal clock

 2. If unused, this pin must tied to VDD or VSS.



1. External signal clock

 2. If unused, this pin must tied to VDD or VSS.



1. External signal clock

 2. If unused, this pin must tied to VDD or VSS.

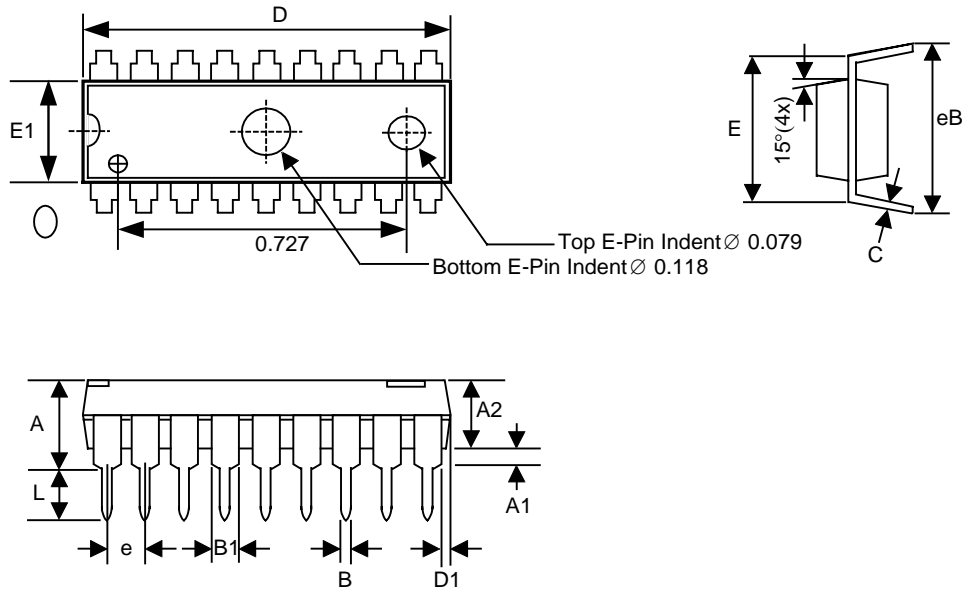


Unit Function Comparison

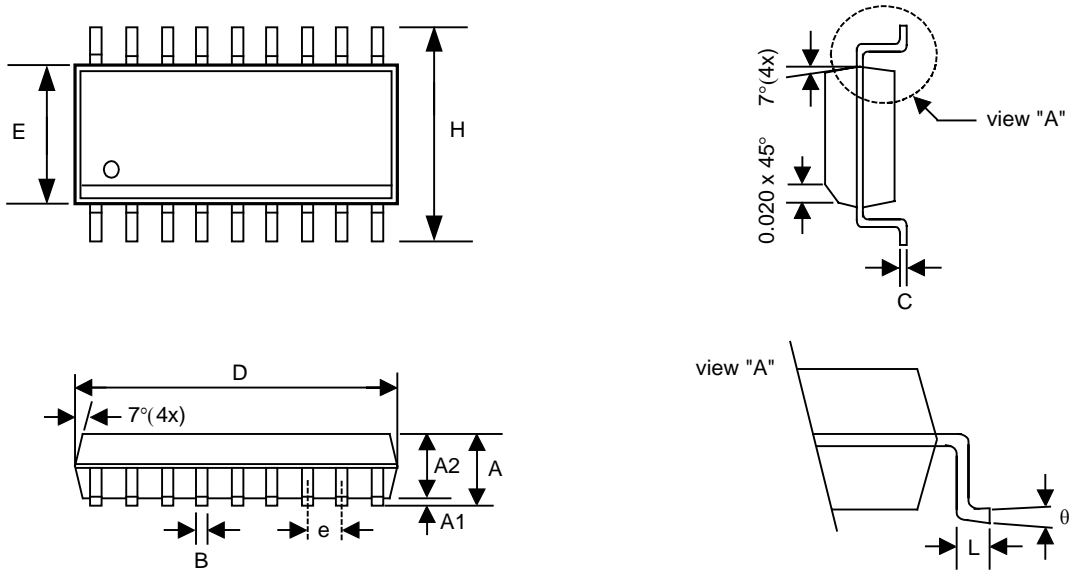
Feature	JA5856F	JA5856
PORTB wake-up	V	X
PORTB pull high/low resistors	V	X
Low voltage reset (1.8V)	V	X
Internal RC oscillation 4MHz/455KHz	V	X

Note:

Legend: V = with function, X = without function

Package Dimension
18 Pin PDIP 300mil for JA5856F


Symbol	Dimension in Millimeters			Dimension in Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	—	—	4.57	—	—	0.180
A1	0.13	—	—	0.005	—	—
A2	—	0.30	3.56	—	—	0.140
B	0.36	0.46	0.56	0.014	—	0.022
B1	1.27	1.52	1.78	0.050	—	0.070
C	0.20	0.25	0.33	0.008	—	0.013
D	22.71	22.96	23.11	0.894	—	0.910
D1	0.43	0.56	0.69	0.017	—	0.027
e	7.62	—	8.26	0.300	—	0.325
E1	6.40	6.50	6.65	0.252	—	0.262
E	—	2.54	—	—	—	—
L	3.18	—	—	0.125	—	—
eB	8.38	—	9.65	0.330	—	0.380

18 Pin PDIP 600mil for JA5856F


Symbol	Dimension in Millimeters			Dimension in Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	—	0.30	0.04	—	0.012
A2	—	2.31	—	—	0.091	—
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	11.35	—	11.76	0.447	—	0.463
E	7.39	7.49	7.59	0.291	0.295	0.299
e	—	1.27	—	—	0.050	—
H	10.01	10.31	10.64	0.394	0.406	0.419
L	0.38	0.81	1.27	0.015	0.032	0.050
θ	0°	—	8°	0°	—	8°

Revision History:

- **Ver. 0.0 – Dec.23.2003 by Kevin Lin**
- **Ver. 0.1 – Dec.24.2003 by Tim Chen**
- **Ver. 0.2 – Jan.17.2004 by Y.C. Lo**
- **Ver. 0.3 – Apr.13.2005 by Alex Wu**
 1. On P.19- 3 deleted Pad Assignment and Coordinates.
 2. On P.19- 3 in Pin Descriptions, added Pin Type and Buffer Type column.
 3. On P.19- 12 in Absolute Maximum Ratings, cancelled some items.
 4. On P.19- 13~14 in Electrical Characteristics, renewed new experimental values.
 5. On P.19- 16, built Unit Function Comparison.