Revision History:

- **Nov.28.2003 – Ver0.0 Initiated by Tim Chen**
- **Dec.01.2003 – Ver0.1 modify by Tim Chen**
- **Dec.11.2003 – Ver0.2 modify by Tim Chen (Green words)**

General Description

JA58572 is an 8-bit micro-controller that employs enhanced CMOS Mask ROM technology with low cost, high speed and high noise immunity. Watchdog Timer, RAM, EPROM, I/O port, power down mode, and real time programmable clock/counter are integrated into this chip. JA58572 contain 33 instructions, all are single cycle except for program branches need take two cycles. On chip memory is available with 2048x14 bits of Mask ROM and 72 bytes of static RAM.

Features

Total 33 single word instructions.

The fast execution time may be 200ns for all single cycle instructions under 20MHz operation.

- Operating voltage range:
  Normal: 2.4V ~ 5.5V / HSXTAL: 3.5V ~ 5.5V
- Operating temperature: 0° C ~ 70° C
- ROM size: 2Kx14 bits
- RAM size: 72 bytes
- Stack: 4 Level stacks
- 8 bits real time clock/counter with 8 bits programmable Pre-scalar.
- Internal Power-on Reset and built-in LVDT circuit (low voltage detector) which selected by option.
- On chip Watch Dog Timer (WDT) based on internal RC oscillator. (18ms@5V)
- Direct and indirect addressing modes for data accessing.
- Sleeping mode for power saving.
  (Less than 1uA @ 5V; **without LVDT**)
  (Less than 3.5uA @ 3V; with LVDT)
- 7 types of oscillators can be selected by options:
  - HSXTAL: High speed crystal oscillator
  - XTAL: Standard crystal oscillator
  - LPXTAL: Low power crystal oscillator
  - RC1: External High-Speed RC oscillator with range of 1MHz to 10MHz. (4MHz - Fc)*
  - RC2: External Low-Speed RC oscillator with range of 32kHz to 1MHz. (455KHz - Fc)*
  - RC3: Internal 4MHz fixed RC oscillator.
  - RC4: Internal **580**kHz fixed RC oscillator.
- Port A, Port B and Port C have 20 I/O pins with independent direction control.
- Port B with pin change wake-up function, which was selected by option.
- Port B with pull high/low resistors, which were selected by option.

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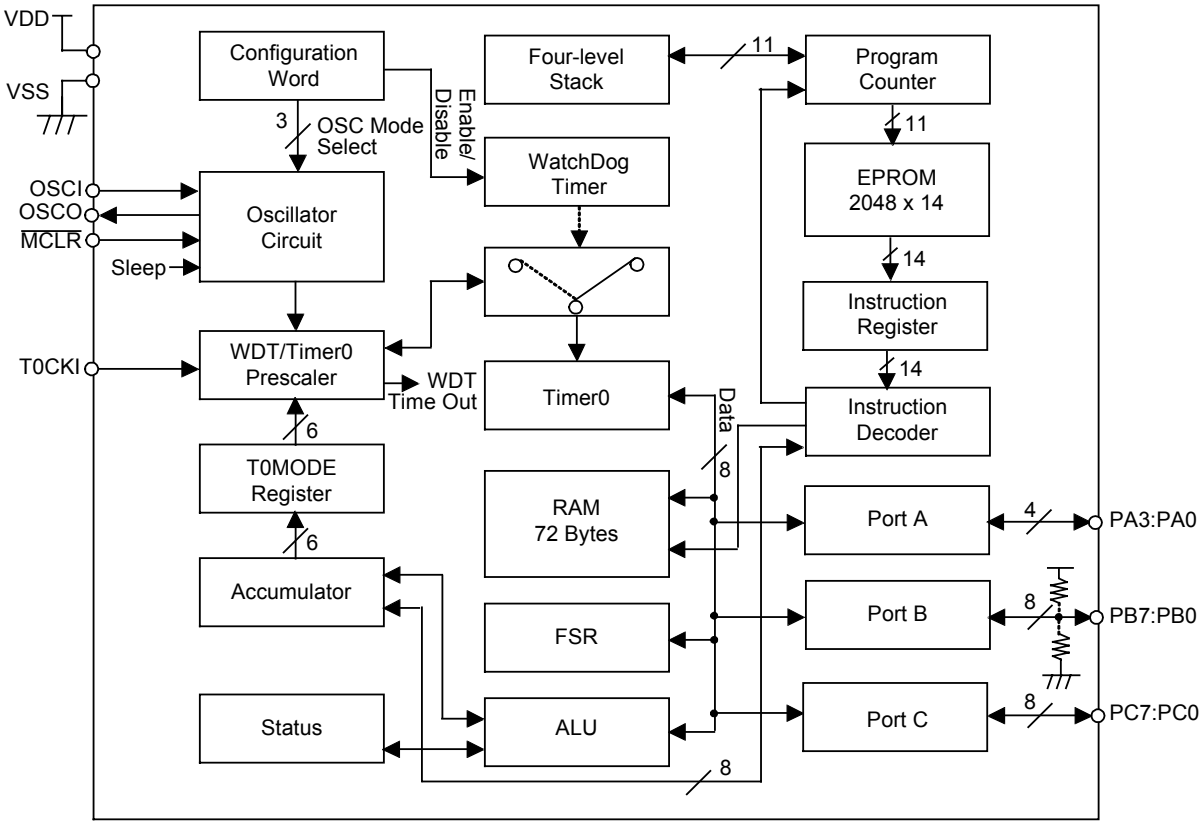
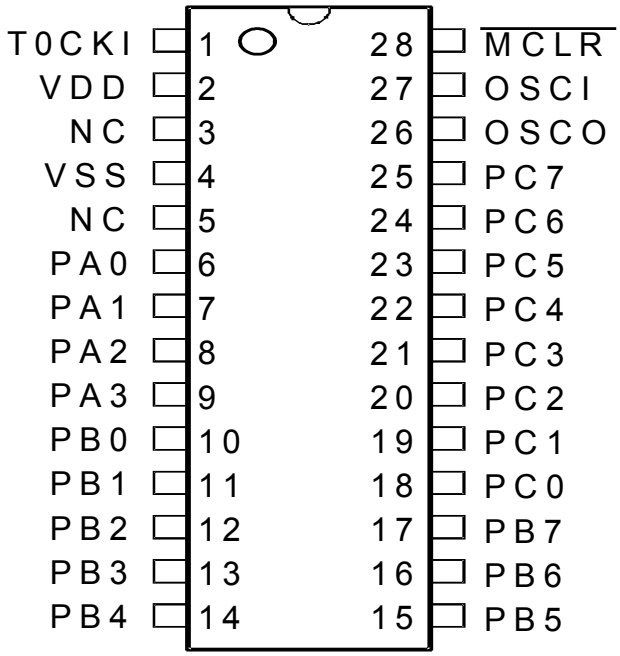
Block Diagram



Pin Assignment (PDIP-28PIN / SOP-28PIN)



JA58572

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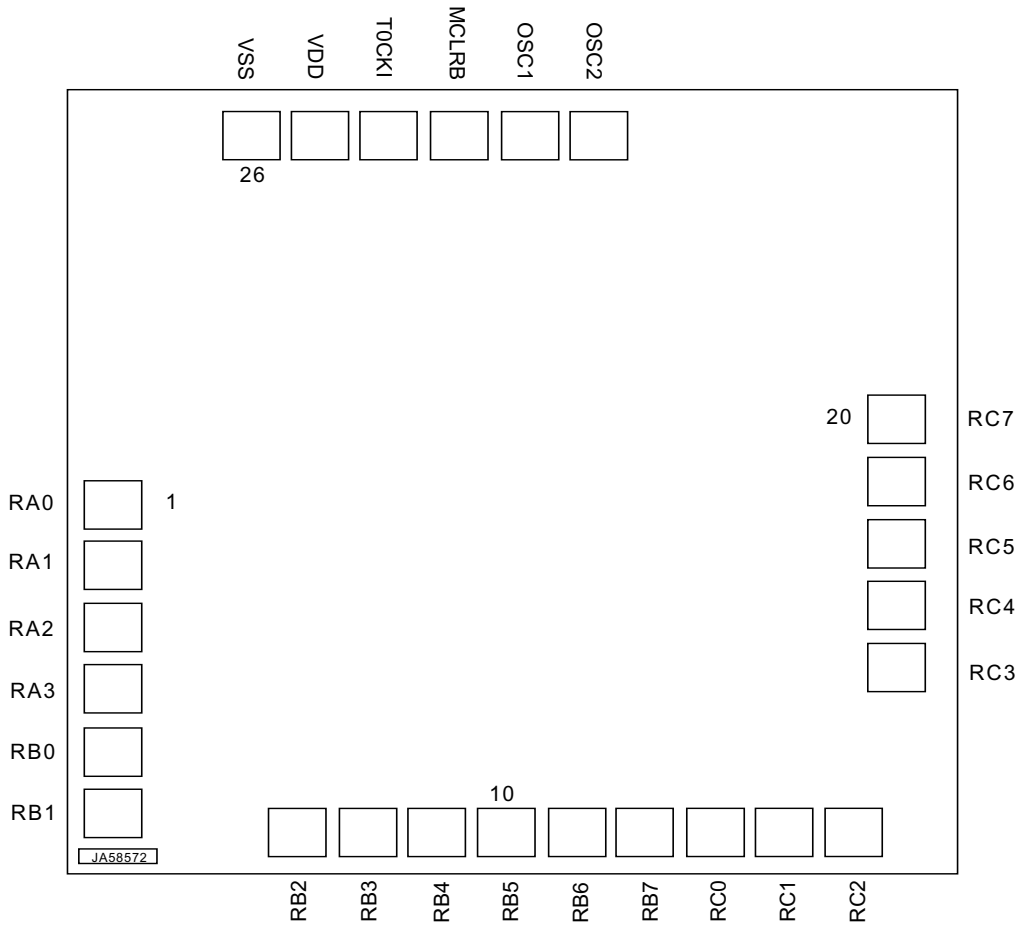
Pad Assignment and Coordinates



Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	RA0	70	652.5	14	RC1	1129.5	70
2	RA1	70	542.7	15	RC2	1239.3	70
3	RA2	70	432.9	16	RC3	1308.8	360.9
4	RA3	70	323.1	17	RC4	1308.8	470.7
5	RB0	70	213.3	18	RC5	1308.8	580.5
6	RB1	70	103.5	19	RC6	1308.8	690.3
7	RB2	360.9	70	20	RC7	1308.8	800.1
8	RB3	470.7	70	21	OSC2	836.1	1299.8
9	RB4	580.5	70	22	OSC1	726.3	1299.8
10	RB5	690.3	70	23	MCLRB	616.5	1299.8
11	RB6	800.1	70	24	T0CKI	506.7	1299.8
12	RB7	909.9	70	25	VDD	396.9	1299.8
13	RC0	1019.7	70	26	VSS	287.1	1299.8
Chip Size: 1380*1370um							

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Pin Descriptions

Pad Name	I/O	Description
OSCI	I	. Oscillator input.
OSCO	O	. Oscillator output. . At RC mode, this pin will output 1/4 frequency of OSCI to denote the cycle rate for instruction.
T0CKI	I	. Input pin of real time counter/clock. If unused, it must be tied to VDD or VSS.
$\overline{\text{MCLR}}$	I	. Input pin for device reset. If this pin is low, the chip is reset. . Build-in LVDT circuit (low voltage detector) which selected by option.
PORTA	I/O	. PA3～PA0 were bi-directional I/O port.
PORTB	I/O	. PB7～PB0 were bi-directional I/O port. . PB7～PB0 with pin change wake-up function which selected by option. . PB7～PB0 pin with pull high/low resistors which selected by option.
PORTC	I/O	. PC7～PC0 were bi-directional I/O port.
VDD	-	. Power supply positive.
VSS	-	. Ground

Register Functional Description

Register Map of JA58572 is depicted as below:

The register map of JA58572				
Address	Description			
	Bank 0	Bank 1	Bank 2	Bank 3
	FSR<6:5>: 00	FSR<6:5>: 01	FSR<6:5>: 10	FSR<6:5>: 11
00H	INAR	Map back to address in Bank 0		
01H	Timer0			
02H	PC			
03H	Status			
04H	FSR			
05H	Port A			
06H	Port B			
07H	Port C			
08H~0FH	General purpose register			
10H~1FH	General purpose register	30H~3FH General purpose register	50H~5FH General purpose register	70H~7FH General purpose register

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INAR (Indirect Address Register): 00H

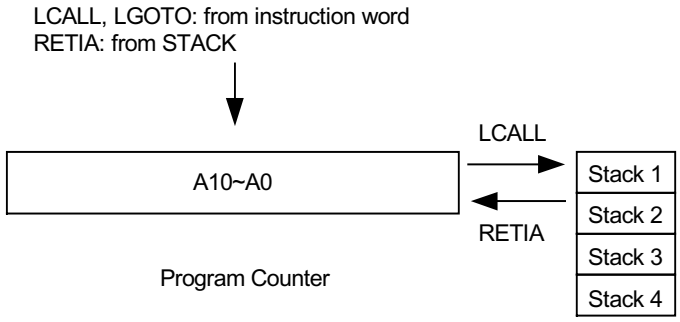
This Register is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction accessing this register can access data pointed by FSR (04H).

Timer0 (8-bit real-time clock/timer): 01H

This register increases by an external signal edge applied to T0CKI pin, or by internal instruction cycle. It can be read or written as any other register.

PC (Program Counter): 02H

This register increases itself along with every instruction cycle, except the following condition specified as below:



Status (Status Register): 03H

Bit	Symbol	Description
0	C	Carry/Borrow bit. ADDAR C = 1 - A carry occurred C = 0 - A carry did not occur SUBAR C = 1 - A borrow did not occur C = 0 - A borrow occurred
1	DC	Half carry/Half borrow bit. ADDAR DC= 1 - A carry from the 4th low order bit of the result occurred DC= 0 - A carry from the 4th low order bit of the result did not occur SUBAR DC= 1 - A borrow from the 4th low order bit of the result did not occur DC= 0 - A borrow from the 4th low order bit of the result occurred
2	Z	Zero bit. Z= 1 - The result of a logic operation is zero Z= 0 - The result of a logic operation is not zero
3	/PD	Power down Flag bit. /PD= 1 - After power-up or by the CLRWDT instruction /PD= 0 - By the SLEEP instruction
4	/TO	Time over Flow flag bit. /TO= 1 - After power-up or by the CLRWDT or SLEEP instruction /TO= 0 - A WDT time-overflow occurred
5~7	-	Reserved

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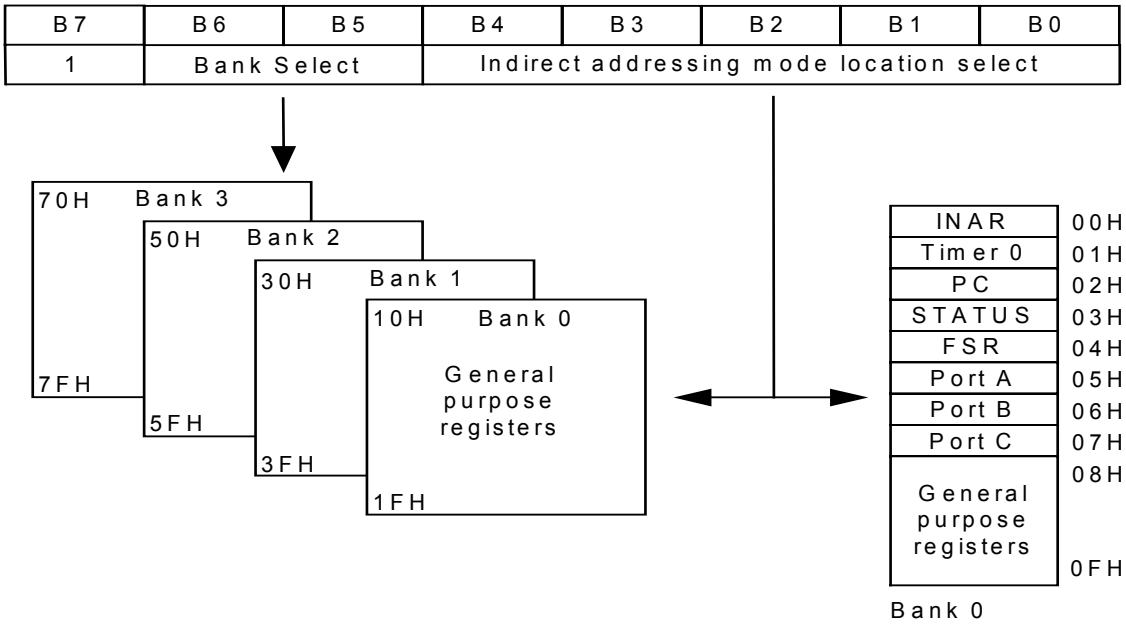
FSR (File select register pointer): 04H

In JA58572, Bit 0~4 are used to select up to 32 registers (address: 00h~1Fh) and Bit 5~6 are Bank Select (Bank 0~3). Using the indirect addressing mode show as below:



Data Memory Configuration for JA58572

PORT A: 05H

PA3～PA0: Bi-directional I/O Register.

PORT B: 06H

PB7～PB0: Bi-directional I/O Register. Each pin of Port B has build-in pull high/low resistor and pin change wake up function that can be select by option independently. Pull high/low resistors and pin change wake up function will enable when user set the I/O pin to input mode and will be disable when it change to output mode. When user use these functions, you must attention something as below：

1. User should select WDT or pin change wake up function individually. In case of pin change wake up enable, WDT must disable. When system wake up by the PORTB pin level change, the instruction located after the SLEEP will be executed.
2. When user want to use the pin change wake up function, it must assign 0FH to Pre-scalar before execute the “SLEEP” instruction. Therefore, user must take care the switching of Pre-scalar.
3. When system in the sleeping mode, the wake up function will happen in case of pin level changed.
4. If user had wake up the chip by I/O pin, please mind the chartering (Bounce) to prevent system mal-function. Please note that the pin change wake-up will delivered by the Rising or Falling signal changed.

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Example:

Configuration word:

WDT**: Disable**
Port B pull high resistors**: Disable**
Port B pull low resistors**: PB0、PB1**
Port B pin change wake up**: PB0**

Source code:

```
        .
        .
        CLRA
        T0MODE              ; Assign Prescaler to Timer0
        IOST    PORTA       ; All pins of Port A were set to output.
        IOST    PORTB       ; All pins of Port B were set to output. Pull low resistor（PB0、PB1）
        .                   ; and pin change wake up function（PB0）will be disable.
        .
        MOVIA   03H         ; PB0 and PB1 were set to input mode. The pull low resistors and
        IOST    PORTB       ; Pin change wake up function were enable
        .
        MOVIA   0FH         ; Assign 0FH to Pre-scalar
        T0MODE
        SLEEP               ; Wait the press of PB0 to wake up the chip
        CLRA
        T0MODE              ; Assign Pre-scalar return Timer0
        LCALL   DELAY       ; Add a delay for bounce
        .
        MOVIA   0FH         ; Assign 0FH to Pre-scalar
        T0MODE
        SLEEP
```

Description:

When the chip was go into sleep mode, the chip is still in the sleep mode even the PB1 had pin level change. If PB0 had pin level change, the chip will wake up and execute the next instruction that “ CLRA ”.

PORT C: 07H

PC7～PC0：Bi-directional I/O Register.

IOST (Control Port I/O Mode Register)

The IOST register is “write-only” and will be set as ‘1’ upon RESET.

IOST Bit-X = 0; I/O Pin-X Set as output mode.
IOST Bit-X = 1; I/O Pin-X Set as input mode.

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T0MODE Register:

T0MODE is a write-only register and the content was be listed as below:

Bit	Symbol	Description		
		Bit Value	Timer Rate	WDT Ratev
2~0	PS2～PS0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	1:2 1:4 1:8 1:16 1:32 1:64 1:128 1:256	1:1 1:2 1:4 1:8 1:16 1:32 1:64 1:128
3	PSC	Prescaler assign bit: = 0 （Timer0） = 1 （WDT）		
4	TE	Timer0 source signal edge select bit: = 0 （Increment when low-to-high transition on T0CKI pin） = 1 （Increment when high-to-low transition on T0CKI pin）		
5	TS	Timer0 source signal select bit: = 0 （Internal instruction clock cycle） = 1 （Transition on T0CKI pin）		
6~7	-	Reserved		

Timer0

Timer0 is an 8-bit timer/counter. The clock source of Timer0 could be come from the internal clock or by an external clock source presented by the T0CKI pin.

To select the internal clock source, bit 5 of the T0MODE register should be clear. In this mode, Timer0 increases by 1 in every instruction cycle (without Pre-scalar).

To select the external clock source, bit 5 of the T0MODE register should be set. In this mode, Timer0 increases by 1 on every falling or rising edge of T0CKI pin which is be controlled by bit 4 of T0MODE register.

Pre-scalar

The 8-bit Pre-scalar may be assigned to either the Timer0 or the WDT through the PSC bit (bit 3 of the T0MODE register). Set this bit to “1” is assigned the Pre-scalar to the WDT. Set this bit to “0” is assigned the Pre-scalar to the Timer0. The PS2:PS0 bits determine the Pre-scale ratio. The Pre-scalar can’t be assigned to both the Timer0 and WDT simultaneously.

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RESET

This device may be reset by one of the following ways:

(1) Power-on Reset: At power-up, this device is kept in a RESET condition for a period of 18ms after the voltage on $\overline{\text{MCLR}}$ pin has reached a logic high level.

(2) $\overline{\text{MCLR}}$ reset (normal operation).

(3) WDT reset (normal operation).

(4) $\overline{\text{MCLR}}$ wake-up (from sleep mode).

(5) WDT wake-up (from sleep mode): Executing the SLEEP instruction can force this device to enter sleep mode (power saving mode). While in sleep mode, the WDT is cleared but keeps running. This device can be awakened by WDT time-out or reset input on $\overline{\text{MCLR}}$ pin.

The contents of registers after reset are listed as below:

Address	Register	Power-On Reset	$\overline{\text{MCLR}}$ or WDT Reset
00h	INAR	xxxx xxxx	uuuu uuuu
01h	Timer0	xxxx xxxx	uuuu uuuu
02h	PC	1111 1111	1111 1111
03h	STATUS	0001 1xxx	000# #uuu
04h	FSR	1xxx xxxx	1uuu uuuu
05h	PORTA	---- xxxx	---- uuuu
06h	PORTB	xxxx xxxx	uuuu uuuu
07h	PORTC	xxxx xxxx	uuuu uuuu
08h-1Fh	General Purpose Register	xxxx xxxx	uuuu uuuu
30h-3Fh	General Purpose Register	xxxx xxxx	uuuu uuuu
50h-5Fh	General Purpose Register	xxxx xxxx	uuuu uuuu
70h-7Fh	General Purpose Register	xxxx xxxx	uuuu uuuu
N/A	Acc	xxxx xxxx	uuuu uuuu
N/A	IOST	1111 1111	1111 1111
N/A	T0MODE	--11 1111	--11 1111

Note:

″x″ = unknown ″u″ = unchanged

″-″ = unimplemented, read as ″0″ ″#″ = refer to the following tables

The STATUS (03H) Register situation for different conditions:

Condition	Status: bit 4 (/TO)	Status: bit 3 (/PD)
$\overline{\text{MCLR}}$ Reset (not during SLEEP)	u	u
$\overline{\text{MCLR}}$ Reset during SLEEP	1	0
WDT Reset (not during SLEEP)	0	1
WDT Reset during SLEEP	0	0

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Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator. This RC oscillator is separated from the RC oscillator of the OSCI pin. That means the WDT keeps running even when the oscillator driver is turned off, such as in sleep mode. During normal operation or in sleep mode, a WDT time-out causes the device reset and the $\overline{TO}$ bit (bit 4 of STATUS register) was cleared.

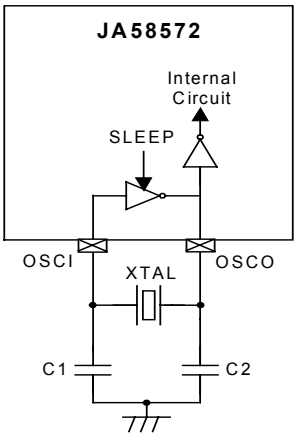
Without Pre-scalar, the WDT time-out period is 18ms. This period can increase by using the Pre-scalar. The division ratio of Pre-scalar is up to 1:128. Thus, the longest time-out period is approximately 2.3s.

Oscillator Configuration

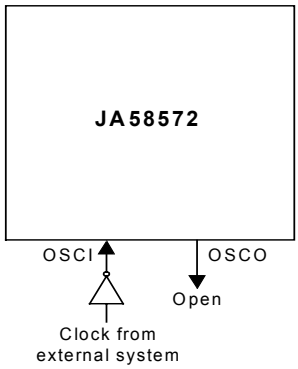
This device supports 7 oscillator modes. Users can select the appropriate mode by compile tool. These oscillator modes offered as:

- HSXTAL: High speed crystal oscillator
- XTAL: Standard crystal oscillator
- LPXTAL: Low power crystal oscillator
- RC1: External Hi-Speed RC oscillator with Range of 1MHz to 10MHz. (4MHz FC)*
- RC2: External Low-Speed RC oscillator with Range of 32kHz to 1MHz. (455kHz FC)*
- RC3: Internal 4MHz fixed RC oscillator.
- RC4: Internal **580**kHz fixed RC oscillator.

XTAL, HFXTAL or LFXTAL modes



(a) Crystal operation (or ceramic resonator)



(b) External clock input operation

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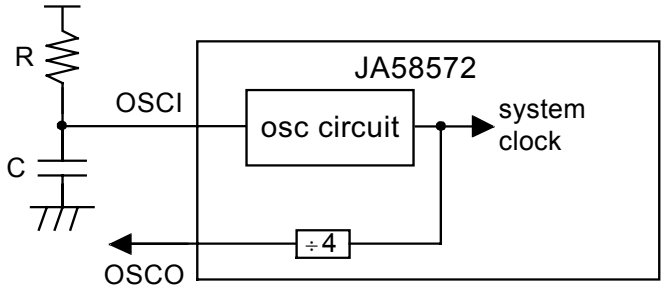
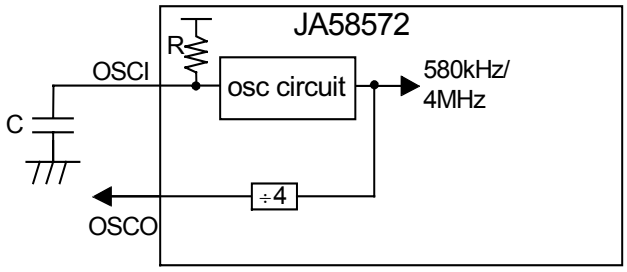
External RC Oscillator Mode



Internal RC Oscillator Mode



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Instruction Table

Mnemonic Operands		Description	Cycles	Instruction Code	Status Affected
BCR	R, bit	Clear bit in R	1	11 11bb brrr rrrr	None
BSR	R, bit	Set bit in R	1	11 10bb brrr rrrr	None
BTRSC	R, bit	Test bit in R and skip if clear	1 or 2(skip)	11 01bb brrr rrrr	None
BTRSS	R, bit	Test bit in R and skip if set	1 or 2(skip)	11 00bb brrr rrrr	None
CLRWDT		Clear Watchdog Timer	1	01 0000 0000 0001	$\overline{TO}$, $\overline{PD}$
T0MODE		Load T0MODE Register	1	01 0000 0000 0010	None
SLEEP		Go into standby mode	1	01 0000 0000 0011	$\overline{TO}$, $\overline{PD}$
IOST	R	Load IOST Register	1	01 0000 0000 0rrr	None
ANDIA	I	AND immediate with Acc	1	00 1001 iiii iiii	Z
XORIA	I	Exclusive OR immediate with Acc	1	00 1000 iiii iiii	Z
MOVIA	I	Move immediate to Acc	1	00 0001 iiii iiii	None
IORIA	I	Inclusive OR immediate with Acc	1	00 0011 iiii iiii	Z
RETIA	I	Return, place immediate in A	2	00 1100 iiii iiii	None
LCALL	I	Call subroutine	2	10 0iii iiii iiii	None
LGOTO	I	Unconditional branch	2	10 1iii iiii iiii	None
NOP		No operation	1	01 0000 0000 0000	None
MOVAR	R	Move Acc to R	1	01 0000 1rrr rrrr	None
COMR	R, d	Complement R	1	01 0010 drrr rrrr	Z
MOVR	R, d	Move R	1	01 0011 drrr rrrr	Z
RRR	R, d	Rotate right R	1	01 1110 drrr rrrr	C
RLR	R, d	Rotate left R	1	01 1100 drrr rrrr	C
SWAPR	R, d	Swap halves R	1	01 1101 drrr rrrr	None
CLRA		Clear Acc	1	01 0001 0000 0000	Z
CLRR	R	Clear R	1	01 0001 1rrr rrrr	Z
INCR	R, d	Increment R	1	01 1000 drrr rrrr	Z
INCRSZ	R, d	Increment R, Skip if 0	1 or 2(skip)	01 1001 drrr rrrr	None
DECR	R, d	Decrement R	1	01 0110 drrr rrrr	Z
DECRSZ	R, d	Decrement R, Skip if 0	1 or 2(skip)	01 0111 drrr rrrr	None
SUBAR	R, d	Subtract Acc from R	1	01 1010 drrr rrrr	C, DC, Z
XORAR	R, d	Exclusive OR Acc with R	1	01 1011 drrr rrrr	Z
ANDAR	R, d	AND Acc with R	1	01 0100 drrr rrrr	Z
ADDAR	R, d	Add Acc and R	1	01 0101 drrr rrrr	C, DC, Z
IORAR	R, d	Inclusive OR Acc with R	1	01 1111 drrr rrrr	Z

Note:

b	: Bit position	WDT	: Watchdog Timer	R	: Register address
i	: Immediate data	Acc	: Accumulator	T0MODE	: T0MODE register
/PD	: Power down flag	/TO	: Time overflow bit	IOST	: I/O port status register
Z	: Zero flag	C	: Carry flag	DC	: Digital carry flag
I	: (i_7 i_6 i_5 i_4 i_3 i_2 i_1 i_0)	R	: (r_6 r_5 r_4 r_3 r_2 r_1 r_0)		

D ∈ [0,1] Destination:
If d is “0”, the result is stored in the Acc register.
If d is “1”, the result is stored back in register R.

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Absolute Maximum Ratings

Parameter	Max.	Unit
Ambient temperature under bias	-55 to +125	°C
Storage temperature	-65°C to +150	°C
Voltage on any pin with respect to VSS	-0.3 to (VDD + 0.3)	V
Voltage on VDD with respect to VSS	-0.3 to +7.5	V
Maximum current out of VSS pin	300	mA
Maximum current into VDD pin	250	mA
Input clamp current, IIK (VI < 0 or VI > VDD)	± 20	mA
Output clamp current, IOK (VO < 0 or VO > VDD)	± 20	mA
Maximum output current sunk by any I/O pin	25	mA
Maximum output current sourced by any I/O pin	25	mA
Maximum current sunk by PORTA, PORTB and PORTC (combined)	200	mA
Maximum current sourced by PORTA, PORTB and PORTC (combined)	200	mA

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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Electrics Characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}		2.4		5.5	V
Input High Voltage	V_{IH}	I/O port, V_{DD}=5V	3.5		5	V
		$\overline{MCLR}$, V_{DD}=5V	4		5	V
Input Low Voltage	V_{IL}	I/O port, V_{DD}=5V	0		1.5	V
		$\overline{MCLR}$, V_{DD}=5V	0		2	V
Output Voltage	V_{OH}	I_{OH}=10mA, V_{DD}=5V		4.5		V
	V_{OL}	I_{OL}=22mA, V_{DD}=5V		0.5		V
HSXTAL: 20MHz; WDT disable; C_{OSCI}=15pF; C_{OSCO}=10pF; LVDT disable; PORTA/B/C: Input/Output Low/Output Low						
Supply Current	I_{DD}	V_{DD}=5.5V		2.9		mA
		V_{DD}=5.0V		2.4		mA
		V_{DD}=4.0V		1.6		mA
		V_{DD}=3.5V		1.2		mA
HSXTAL: 12MHz; WDT disable; C_{OSCI}=15pF; C_{OSCO}=10pF; LVDT disable; PORTA/B/C: Input/Output Low/Output Low						
Supply Current	I_{DD}	V_{DD}=5.5V		2.1		mA
		V_{DD}=5.0V		1.7		mA
		V_{DD}=4.0V		1.1		mA
		V_{DD}=3.5V		0.8		mA
XTAL: 12MHz; WDT disable; C_{OSCI}=15pF; C_{OSCO}=10pF; LVDT disable; PORTA/B/C: Input/Output Low/Output Low						
Supply Current	I_{DD}	V_{DD}=5.5V		2.1		mA
		V_{DD}=5.0V		1.7		mA
		V_{DD}=4.0V		1.1		mA
		V_{DD}=3.0V		0.6		mA
		V_{DD}=2.4V		0.4		mA
XTAL: 4MHz; WDT disable; C_{OSCI}=15pF; C_{OSCO}=10pF; LVDT disable; PORTA/B/C: Input/Output Low/Output Low						
Supply Current	I_{DD}	V_{DD}=5.5V		1.4		mA
		V_{DD}=5.0V		1.1		mA
		V_{DD}=4.0V		0.6		mA
		V_{DD}=3.0V		0.3		mA
		V_{DD}=2.4V		0.2		mA

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Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
LPXTAL: 32kHz; WDT disable; C_{OSCI}=15pF; C_{OSCO}=10pF; LVDT disable; PORTA/B/C: Input/Output Low/Output Low							
Supply Current	I_{DD}	V_{DD}=5.5V			120		uA
		V_{DD}=5.0V			75		uA
		V_{DD}=4.0V			30		uA
		V_{DD}=3.0V			8		uA
		V_{DD}=2.4V			3		uA
External RC mode; Fc=4MHz; R=100kOhm; C_{OSCI}=100pF;							
Supply Current	I_{DD}	V_{DD}=5.5V	F=0.997MHz		285		uA
		V_{DD}=5.0V	F=1.01MHz		235		uA
		V_{DD}=4.0V	F=1.03 MHz		150		uA
		V_{DD}=3.0V	F=1.07 MHz		80		uA
		V_{DD}=2.4V	F=1.10 MHz		53		uA
External RC mode; Fc=4MHz; R=47kOhm; C_{OSCI}=100pF							
Supply Current	I_{DD}	V_{DD}=5.5V	F=2.02 MHz		430		uA
		V_{DD}=5.0V	F=2.03 MHz		365		uA
		V_{DD}=4.0V	F=2.06 MHz		245		uA
		V_{DD}=3.0V	F=2.12 MHz		145		uA
		V_{DD}=2.4V	F=2.10 MHz		100		uA
External RC mode; Fc=4MHz; R=22kOhm; C_{OSCI}=100pF							
Supply Current	I_{DD}	V_{DD}=5.5V	F=4.05 MHz		720		uA
		V_{DD}=5.0V	F=4.05 MHz		620		uA
		V_{DD}=4.0V	F=4.07 MHz		435		uA
		V_{DD}=3.0V	F=4.05 MHz		270		uA
		V_{DD}=2.4V	F=3.82 MHz		185		uA
External RC mode; Fc=4MHz; R=10kOhm; C_{OSCI}=100pF							
Supply Current	I_{DD}	V_{DD}=5.5V	F=7.66 MHz		1245		uA
		V_{DD}=5.0V	F=7.64 MHz		1080		uA
		V_{DD}=4.0V	F=7.54 MHz		775		uA
		V_{DD}=3.5V	F=7.42 MHz		625		uA

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Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
External RC mode; Fc=455kHz; R=6.4MOhm; C_{OSCI} =100pF							
Supply Current	I_{DD}	V_{DD}=5.5V	F=29.7 kHz		100		uA
		V_{DD}=5.0V	F=29.9 kHz		75		uA
		V_{DD}=4.0V	F=30.1 kHz		35		uA
		V_{DD}=3.0V	F=30.7 kHz		10		uA
		V_{DD}=2.4V	F=30.8 kHz		3		uA
External RC mode; Fc=455kHz; R=390kOhm; C_{OSCI} =100pF							
Supply Current	I_{DD}	V_{DD}=5.5V	F=414 kHz		145		uA
		V_{DD}=5.0V	F=417 kHz		115		uA
		V_{DD}=4.0V	F=428 kHz		65		uA
		V_{DD}=3.0V	F=437 kHz		35		uA
		V_{DD}=2.4V	F=430 kHz		20		uA
External RC mode; Fc=455kHz; R=150kOhm; C_{OSCI} =100pF							
Supply Current	I_{DD}	V_{DD}=5.5V	F=943 kHz		210		uA
		V_{DD}=5.0V	F=949 kHz		175		uA
		V_{DD}=4.0V	F=966 kHz		110		uA
		V_{DD}=3.0V	F=972 kHz		65		uA
		V_{DD}=2.4V	F=937 kHz		40		uA
External RC mode; Fc=455kHz; R=68kOhm; C_{OSCI} =100pF							
Supply Current	I_{DD}	V_{DD}=5.5V	F=1898 kHz		345		uA
		V_{DD}=5.0V	F=1904 kHz		290		uA
		V_{DD}=4.0V	F=1915 kHz		195		uA
		V_{DD}=3.0V	F=1877 kHz		120		uA
		V_{DD}=2.4V	F=1755 kHz		80		uA

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Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal RC mode; Fc=**580**kHz; Cosc1=100pF							
Supply Current	IDD	VDD=5.5V	F=562 kHz		165		uA
		VDD=5.0V	F=570 kHz		135		uA
		VDD=4.0V	F=590 kHz		80		uA
		VDD=3.0V	F=608 kHz		40		uA
		VDD=2.4V	F=600 kHz		27		uA
Internal RC mode; Fc=4MHz; Cosc1=100pF							
Supply Current	IDD	VDD=5.5V	F=4.30 MHz		720		uA
		VDD=5.0V	F=4.34 MHz		610		uA
		VDD=4.0V	F=4.45 MHz		430		uA
		VDD=3.0V	F=4.54 MHz		280		uA
		VDD=2.4V	F=4.39 MHz		190		uA
Power down mode; WDT disable **(without LVDT)**							
Supply Current	IDD	VDD=5.5V	-			1	uA
		VDD=5.0V	-			1	uA
		VDD=4.0V	-			1	uA
		VDD=3.0V	-			1	uA
		VDD=2.4V	-			1	uA
Power down mode; WDT enable **(without LVDT)**							
Supply Current	IDD	VDD=5.5V	-		15		uA
		VDD=5.0V	-		12		uA
		VDD=4.0V	-		7		uA
		VDD=3.0V	-		4		uA
		VDD=2.4V	-		3		uA
Internal WDT RC; Pre-scalar = 1:1							
Watch Dog Timer	TWDT	VDD=5.5V			17.6		ms
		VDD=5.0V			18		ms
		VDD=4.0V			19.2		ms
		VDD=3.0V			20.7		ms
		VDD=2.4V			21		ms

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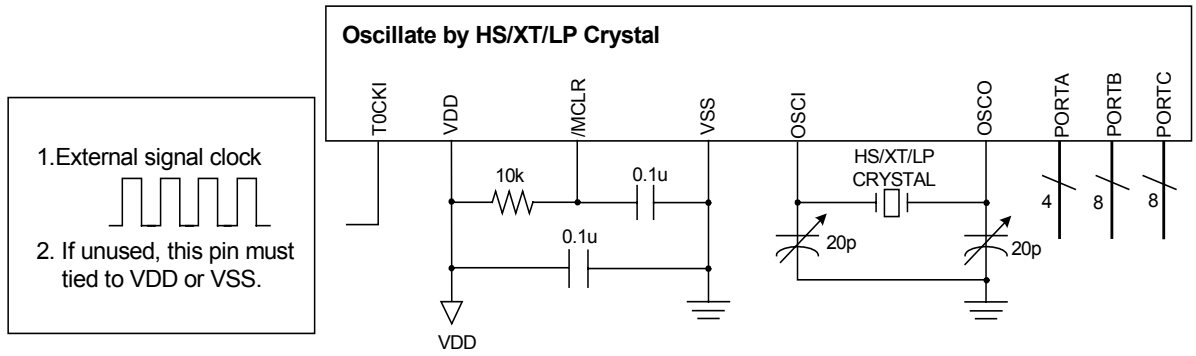
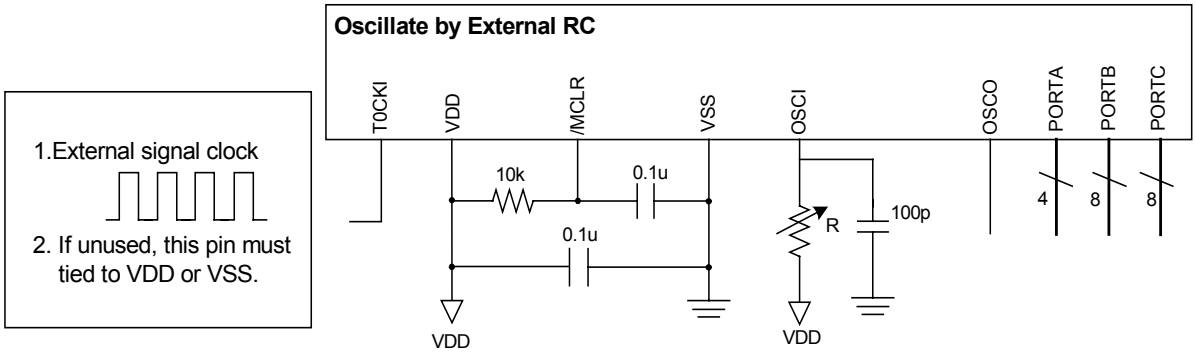
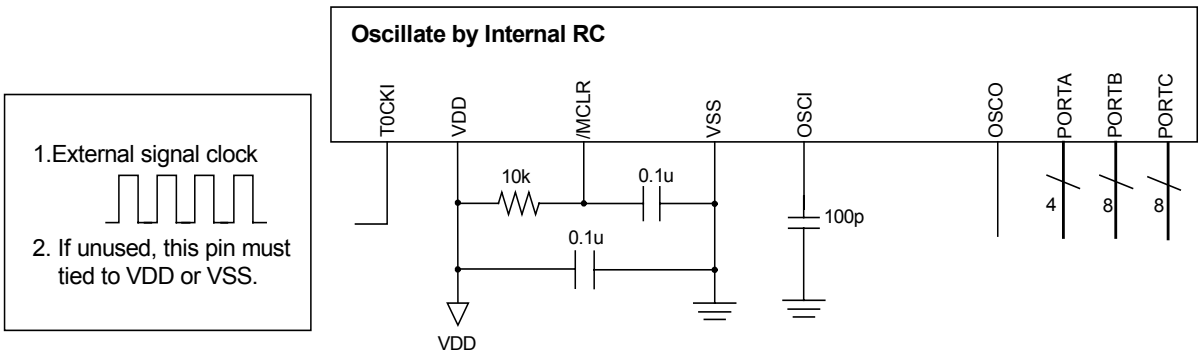
Application Circuit







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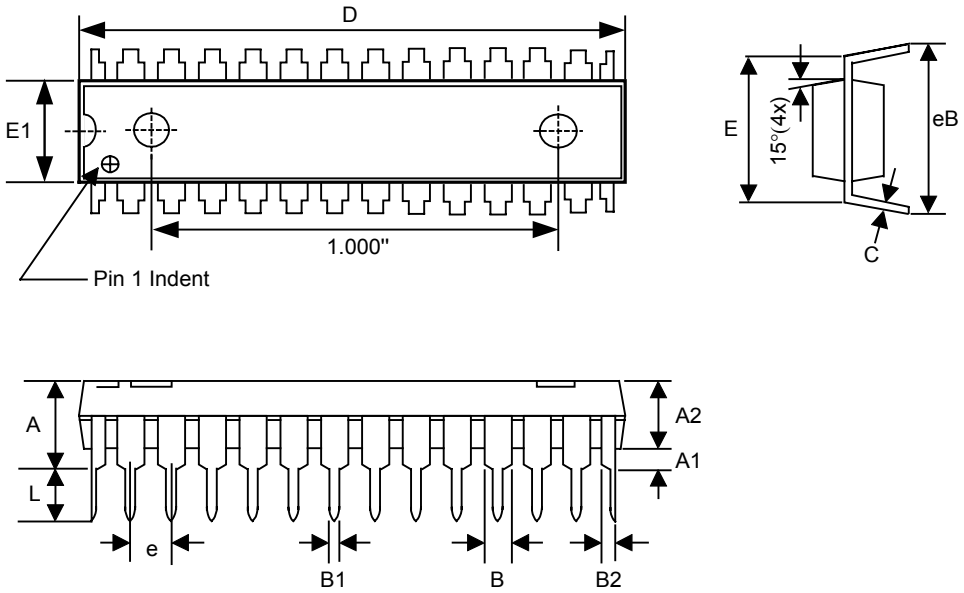
Package Dimension

28 Pin PDIP 300mil for JA58572



Symbol	Dimension in Millimeters			Dimension in Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	—	—	4.57	—	—	0.180
A1	0.38	—	—	0.015	—	—
A2	—	3.30	3.56	—	0.130	0.140
B	1.02	—	1.65	0.004	—	0.065
B1	0.41	—	0.58	0.016	—	0.023
C	0.71	—	1.12	0.028	—	0.044
D	0.20	0.25	0.33	0.008	0.010	0.013
D1	35.13	35.18	35.43	1.383	1.385	1.395
e	7.87	8.31	8.38	0.310	0.327	0.330
E1	7.26	7.32	7.52	0.284	0.288	0.296
E	—	2.54	—	—	0.100	—
L	3.18	—	—	0.125	—	—
eB	8.64	—	9.65	0.340	—	0.380

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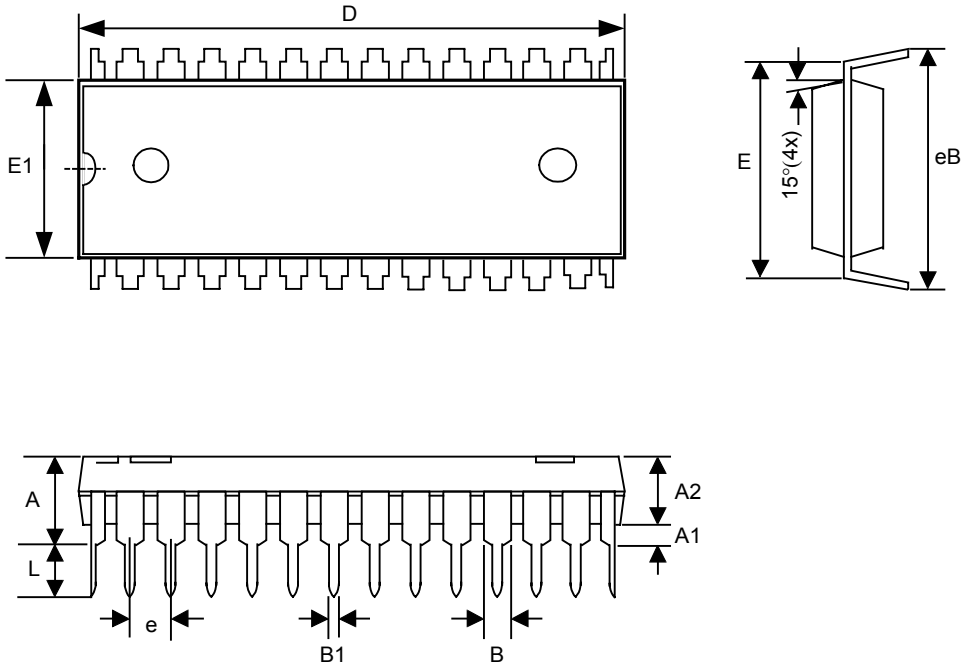
28 Pin PDIP 600mil for JA58572



Symbol	Dimension in Millimeters			Dimension in Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	—	—	5059	—	—	0.220
A1	0.38	—	—	0.015	—	—
A2	3.81	3.94	4.06	0.150	0.155	0.160
B	—	1.52	—	—	0.06	—
B1	—	0.46	—	—	0.018	—
D	36.96	37.08	37.34	1.455	1.460	1.470
E	—	15.24	—	—	0.600	—
E1	13.72	13.84	13.97	0.540	0.545	0.550
e	—	2.54	—	—	0.100	—
L	3.18	—	—	0.125	—	—
eB	16.00	16.51	17.02	0.630	0.650	0.670

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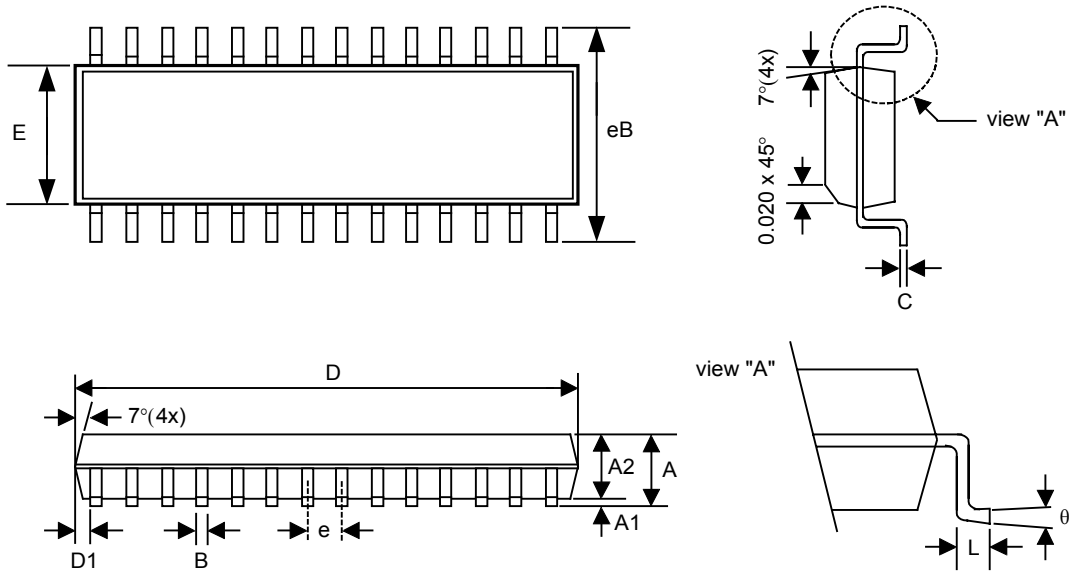
28 Pin SOP for JA58572



Symbol	Dimension in Millimeters			Dimension in Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	—	2.488	2.743	—	0.098	0.108
A1	0.152	—	—	0.006	—	—
A2	2.210	2.336	2.464	0.087	0.091	0.097
B	0.305	0.406	0.508	0.012	0.016	0.020
C	0.204	0.254	0.304	0.008	0.010	0.012
D	17.78	17.91	18.42	0.700	0.705	0.725
E	3.366	7.493	7.62	0.290	0.295	0.300
e	1.219	1.270	1.321	0.048	0.050	0.052
eB	10.26	10.42	10.57	0.404	0.410	0.416
L	0.635	—	—	0.025	—	—
θ	0°	4°	8°	0°	4°	8°
D1	0.356	0.508	—	0.014	0.020	—

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